0 Operation principle of power semiconductors

0.1 Basic switching processes

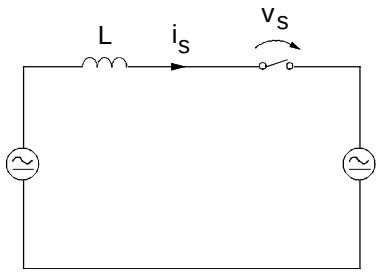
Apart from a few special applications, power semiconductors are mainly used in switching applications. This leads to some basic principles and operation modes which apply to all power electronics circuitries. The most important goal of all efforts in developing the product range of power semiconductors and their applications in circuits is to reach minimum power losses. Limit conditions for the ideal switch are characterized as follows:

ideal switch

- On-state: $v_s = 0$; $-\infty < i_s < \infty$
- Off-state: $i_s = 0$; $-\infty < v_s < \infty$
- Switching behaviour: no conversion of energy during active turn-on/ turn-off

The application of such ideal switches and, consequently, the use of power semiconductors is therefore subject to restrictive switching conditions.

Switches in inductive circuits (impressed current)
A switch applied in an inductive circuit (Fig. 0.1) can actively be turned on, i.e. it can be turned on at any time. There is no power loss under the condition of infinite switching time, since the bias voltage may drop directly over the line inductance.
If the circuit is live, turn-off is not possible without conversion of energy, since the energy stored in L has to be converted. For this reason, turn-off of the switch without any energy conversion is only possible if $i_s = 0$. This is also called passive turn-off, since the switching moment is dependent on the current flow in the circuit. A switch that is running under these switching conditions is called zero-current-switch (ZCS).

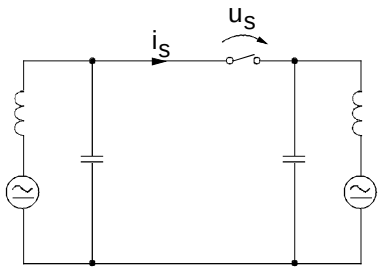


- On-state: $v_s = 0$; $-\infty < i_s < \infty$
- Off-state: $i_s = 0$; $-\infty < v_s < \infty$
- Switching behaviour: active turn-on at $|v_s| > 0$
  passive turn-off at $i_s = 0$

Figure 0.1 Switch in an inductive circuit

Switch between capacitive nodes (impressed voltage)

Nondissipative turn-on of a switch under a impressed voltage is only possible if $v_s = 0$. This is called passive turn-on, since the voltage waveform and, thus, the zero crossing is determined by the outer circuit. Active turn-off, however, will be possible at any time. Switches running under those switching conditions are called zero-voltage-switches (ZVS).



- On-state: $v_s = 0$; $-\infty < i_s < \infty$
- Off-state: $i_s = 0$; $-\infty < v_s < \infty$
- Switching behaviour: active turn-off at $|i_s| > 0$
  passive turn-on at $v_s = 0$

Figure 0.2 Switch between capacitive nodes

Figure 0.3 shows current and voltage waveforms during the basic switching processes described above. The use of real power semiconductors as switches will lead to the following conditions.

Before active turn-on, the current-transferring semiconductor is under positive voltage. Voltage may drop, if, triggered by the controller, the current increases by a certain rate given by the turn-on mechanism of the power semiconductor.
This turn-on mechanism together with the series inductance is limiting the current rise and voltage distribution within the circuit between power semiconductor and inductance. Turn-on power losses of the given power semiconductor are diminished to a minimum value by increase of inductance.
During passive turn-off of a live power semiconductor carrying current in positive direction, current drops to zero due to the voltage polarity of the outer circuit. Current is conducted back as reverse current by the charge carriers still stored in the semiconductor until the semiconductor has recovered its blocking capability to take up the negative circuit voltage.

Active turn-off of a live power semiconductor will, first of all, produce a voltage rise in positive direction triggered by the controller. Then, the effective parallel capacitance will take over the current flow given by the turn-off mechanism of the power semiconductor. The energy loss caused by the turn-off procedure is reduced by the increase of capacitance for the given power semiconductor.

A passively switched power semiconductor is under negative voltage before turn-on. If this voltage changes polarity due to processes in the outer circuit, the power semiconductor will take up current in positive direction, which will lead to turn-on overvoltage in case of impressed current rise.

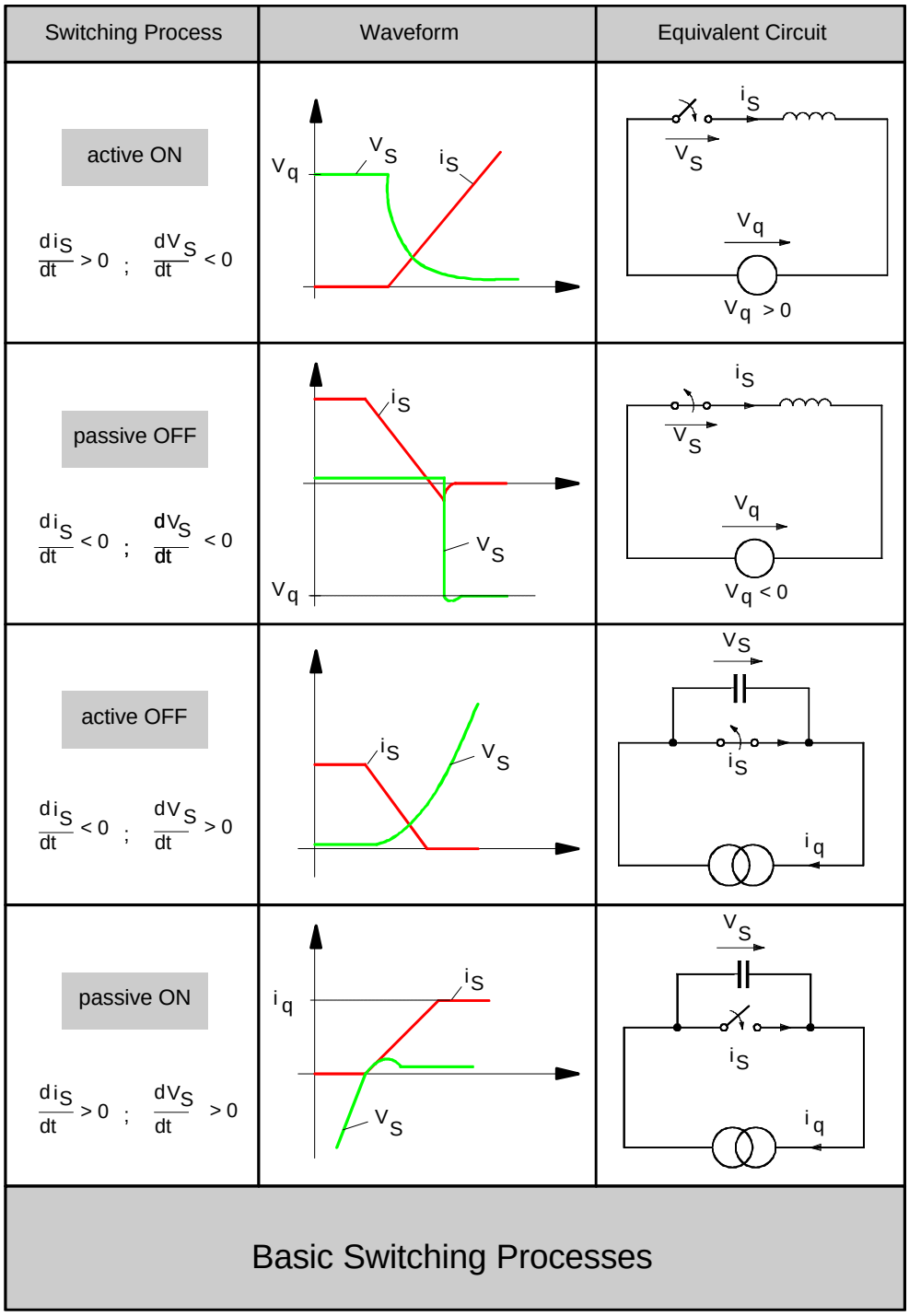


Figure 0.3 Basic switching processes

Every power electronic system works according to two basic function principles:

- firstly, turn-on and turn-off of connection leads between energy exchanging circuitries by means of one switch each - called **cyclic switching** of single switches

and

- secondly, alternating switching of two switches each, alternating current- and voltage-carrying - called **commutation**.

Both basic principles may be integrated into one circuit and the circuit split into several different operation modes.

0.2 Operation principle of power semiconductors

The operation principle of power semiconductors is clearly defined in the previously explained active and passive switching procedures during cyclic switching of single switches and inductive or capacitive commutation. Figure 0.4 shows a summary of the relationships between current and voltage during the different possible switching procedures.

Hard switching (HS, Figure 0.7)

Hard turn-on is characterized by an almost total v_K voltage drop over the current-carrying switch S_1 at a current commutation time t_K causing considerable power loss peaks within the power semiconductor. Commutation inductance is at its minimum value at that moment, i.e. the turned on semiconductor determines the current increase. Current commutation is terminated by passive turn-off of switch S_2. Commutation and switching time are almost identical.
In case of hard turn-off, voltage over S_1 increases up to a value exceeding voltage v_K while current continues flowing. Only then current commutation is started by passive turn-on of S_2. The commutation capacitance is very low, so that the voltage increase is mainly determined by the features of the power semiconductor. Therefore, switching and commutation time are almost the same and there are very high power loss peaks within the switch.

Soft switching (ZCS, ZVS, Figures 0.8 and 0.9)

In the case of soft turn-on of a zero-current-switch the switch voltage will drop relatively fast to the forward voltage drop value, if L_K has been dimensioned sufficiently. Thus, power losses in the switches are almost avoidable during current commutation. Current increase is determined by the commutation inductance L_K. Current commutation is terminated by passive turn-off of S_2, which will cause an increase of the commutation time t_K compared to the switching time t_S.
Active turn-off of S_1 will initialize soft turn-off of a zero-voltage-switch. The decreasing switch current commutates to the capacitance C_K and initializes the voltage commutation process. C_K is bigger than C_{Kmin}, which has considerable influence on the voltage increase rate. Power losses will be reduced by the delayed voltage increase at the switch.

Resonant switching (ZCRS, ZVRS, Figures 0.10 and 0.11)

We are talking about resonant turn-on, if a zero-current-switch is turned on at that moment when current i_L almost drops to zero. Switching losses are still reduced compared to soft switching. Since the switch cannot actively determine the time of zero-current crossing, the controllability is slightly restricted.
On the other hand, we are talking about resonant turn-off of a zero-voltage-switch, if the commutation voltage almost drops to zero during the turn-off process. Once again, switching losses are reduced compared to soft turn-off of the zero-voltage-switch accepting the loss of one control possibility.

Neutral switching (NS, Figure 0.12)

If the switch voltage as well as the switch current are zero at the moment of switching, this is called neutral switching. This is mostly the case with the application of diodes.

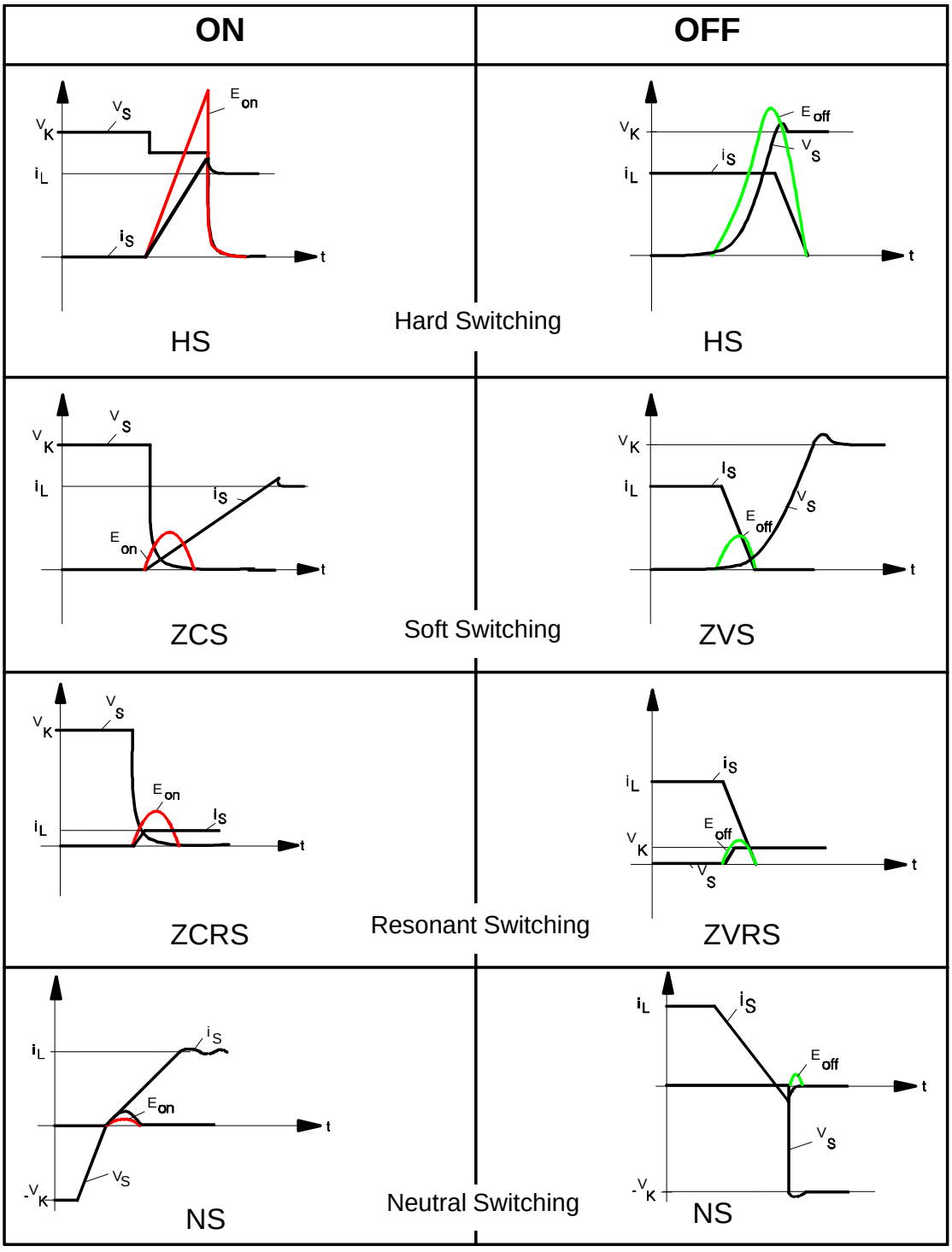


Figure 0.4 Switching procedures (v_K = driving commutation voltage, i_L = load current)

0.3 Power electronic switches

A power electronic switch integrates a combination of power electronic components or power semiconductors and a driver for the actively switchable power semiconductors. The internal functional correlations and interactions of this integrated system determine several characteristics of the switch.

Figure 0.5 shows the power electronic switch system with its interfaces to the external electric circuitry (normally high potential) and to the control unit (information processing, auxiliary power supply). The necessary potential separation is supported by optical or inductive transmitters.
The possible combinations of power semiconductors differing from each other by switch current and voltage direction are shown in Figure 0.6.

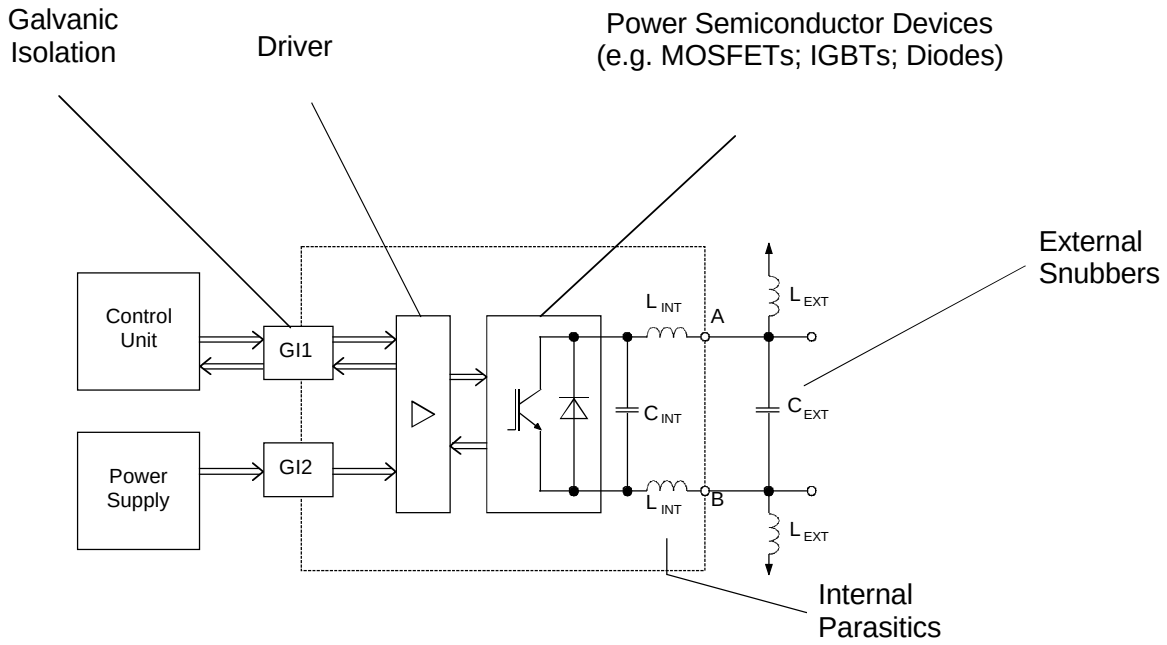
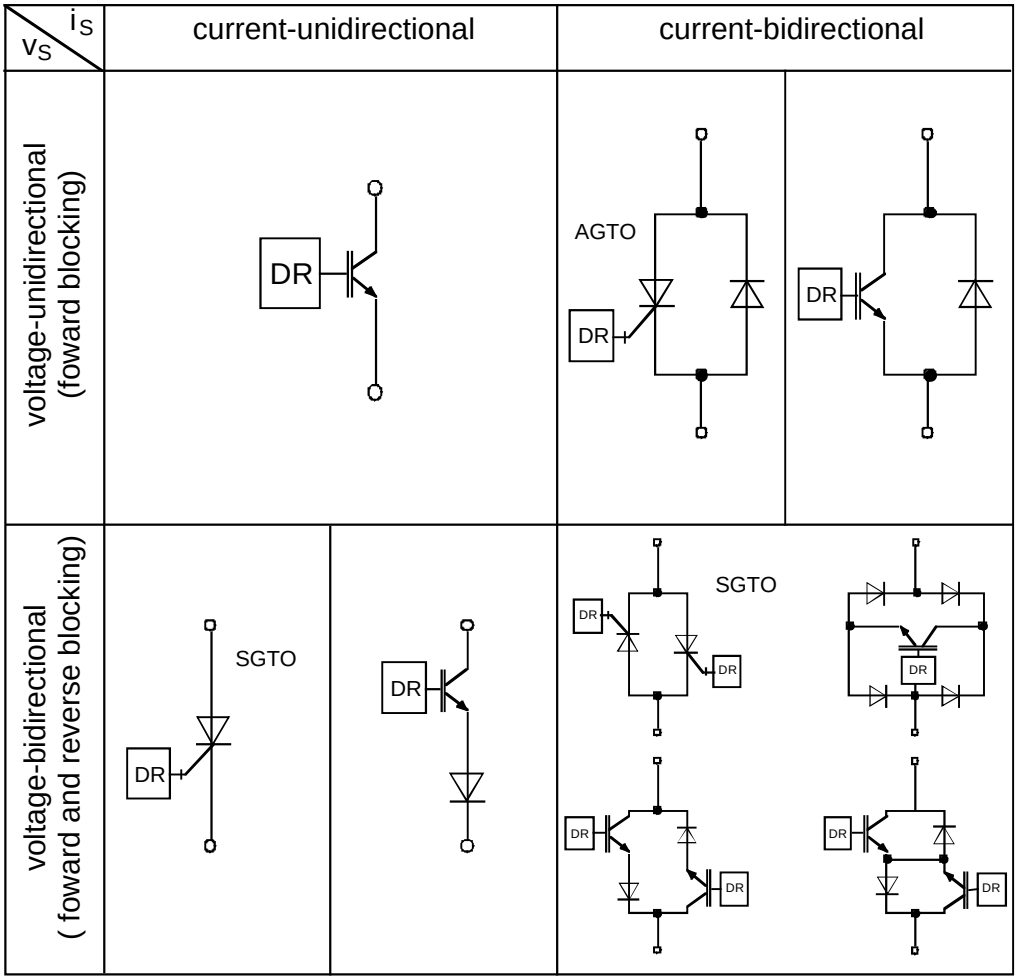


Figure 0.5 Power electronic switch system

On the one hand, the parameters of a complete switch result from the switching behaviour of the semiconductor which, by design of the semiconductor chips, has to be adapted to the operation mode of the whole switch. On the other hand, the driver unit is responsible for all main parameters of the switch and takes charge the most important protectional functions.



SGTO = symmetrical GTO

AGTO = asymmetrical GTO

Figure 0.6 Possible combinations of power semiconductors

Basic types of power electronic switches

Due to the operational principles of power semiconductors, which are mainly responsible for the dominant characteristics of the circuits, power electronic switches may be split up into the following basic types. The main current and voltage directions result from individual circuit requirements.

Hard switch (HS, Figure 0.7)

Except for the theoretical case of pure ohmic load, a single switch with hard turn-on and turn-off switching behaviour can be used only together with a neutrally switchable power semiconductor in a commutation circuit with a minimum passive energy store (C_{Kmin}; L_{Kmin}). Compared to the neutral switch which does not have any control possibility, the hard switch may be equipped with two control possibilites, namely individually adjustable turn-on and turn-off. Figure 0.7 shows the possible switch configurations. As for the symmetrical switch arrangements, only one alternating current-carrying switch will operate acitvely with two control possibilities while the other one switches neutrally.

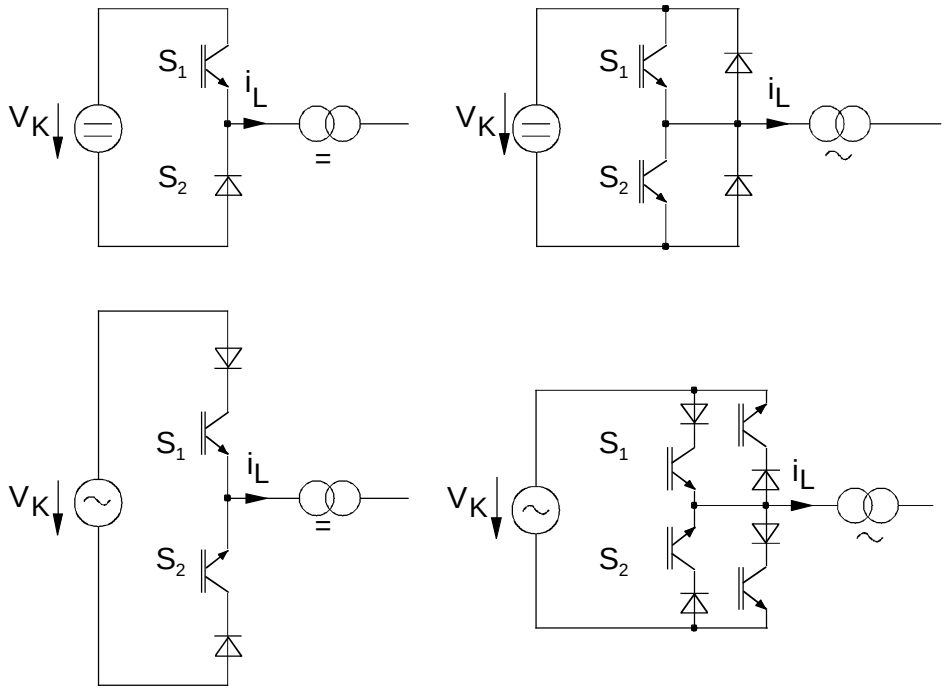


Figure 0.7 HS commutation circuits

Zero-current-switch (ZCS, Figure 0.8)

Power semiconductors in zero-current-switches are turned on actively and turned off passively. Accepting the loss of one control possibility compared to HS, active switching may proceed with considerably decreased power losses due to sufficient series inductance. Figure 0.8 shows the possible switch configurations of a ZCS in an equivalent commutation circuit, which are also applicable in circuits with cyclic switching without commutation. Such circuits are characterized by continuous inductive commutation processes, i.e. active turn-on is followed by passive turn-off.

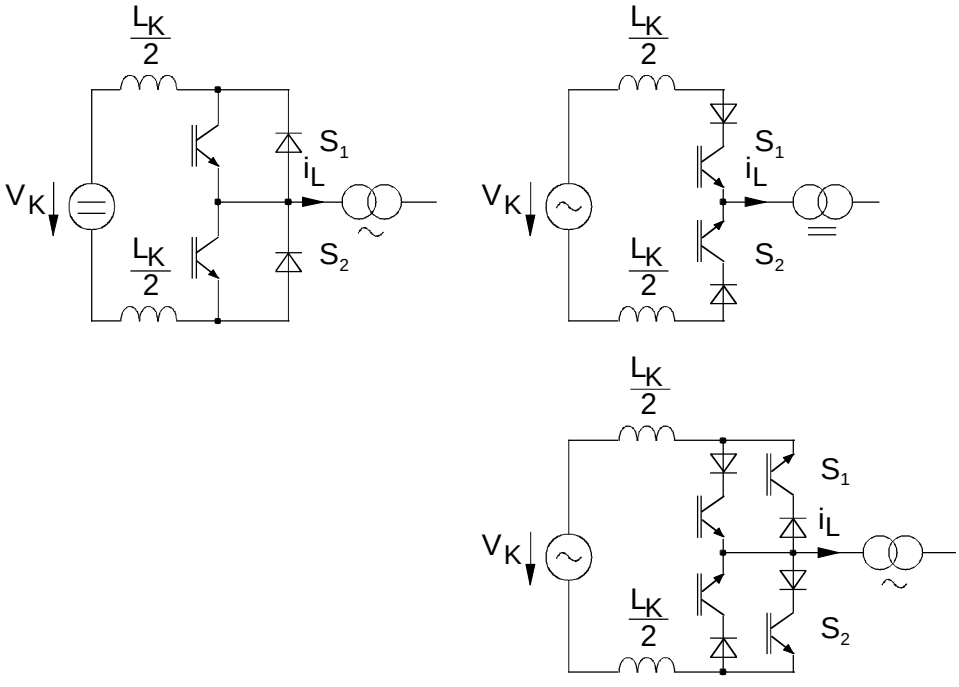


Figure 0.8 ZCS commutation circuits

Zero-voltage-switch (ZVS, Figure 0.9)

Zero-voltage-switches are designed in such a way that they may be turned off actively and turned on passively when the switch voltage drops to zero. Active turn-off may just cause very low losses, if the parallel capacitance has been chosen high enough. Compared to HS a decrease of power losses is possible by accepting the loss of control possibility. Figure 0.9 shows the possible switching arrangements of zero-voltage-switches in capacitive commutation circuits. However, zero-voltage-switches may also be applied in circuits without commutation, where active turn-off and passive turn-on of the same switch are alternating.

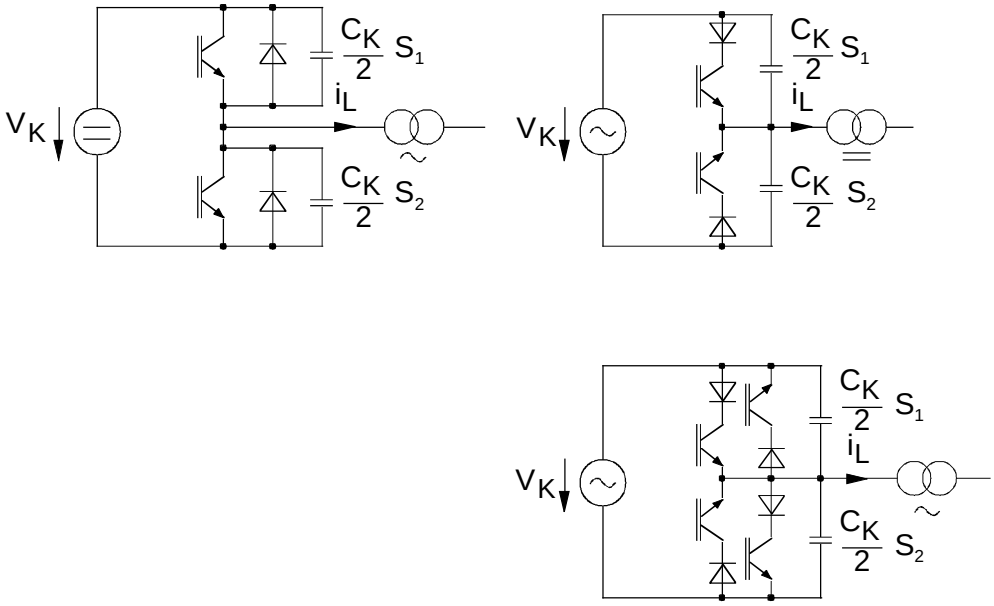


Figure 0.9 ZVS commutation circuits

Zero-current-resonant-switch (ZCRS, Figure 0.10)

If a zero-current-switch is controlled in such a way that active turn-on is started exactly when current is at zero-crossing, there will be no current commutation. Consequently, even if there is a minimum commutation inductance, the power losses are lower than in zero-current-switches; they are just caused by the still necessary change in charge of the junction capacitances of the power semiconductors. The further power loss reduction compared to ZCS demands, at the same time, another loss of controllability, since the turn-on moment is not controllable, but is triggered by the zero-current-crossing given by the outer circuitry. Energy flow can only be controlled indirectly with ZCRS, either conducting or rejecting several current cycles.

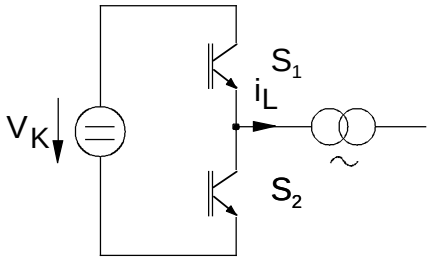


Figure 0.10 ZCRS commutation circuit

Zero-voltage-resonant-switch (ZVRS, Figure 0.11)

This basic type of switch is a borderline case of the ZVS. If a ZVS actively turns off exactly at zero-crossing of the applied commutation alternating voltage, the increasing switch voltage will trigger the current commutation process. Even in the case of minimum commutation capacitance power losses are reduced, however at the expense of active controllability. Indirect control is also possible with the ZVRS, if several commutation voltage cycles are connected through or rejected.

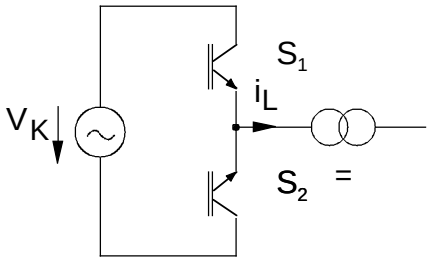


Figure 0.11 ZVRS commutation circuit

Neutral switch (NS, Figure 0.12)

A commutation process is finished by neutral turn-on or turn-off of a neutral switch. In this case current and voltage drop to zero. Generally, a diode already includes these features. A neutral switch with actively switchable power semiconductors owes this special features to a special driver circuit.

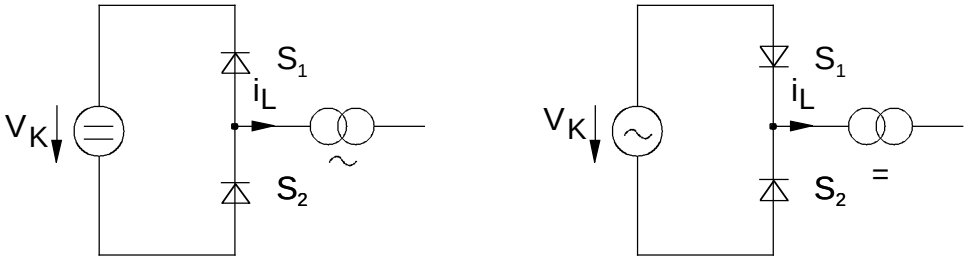


Figure 0.12 NS commutation circuits

Figure 0.13 shows a summary of all basic types of power electronic switches. The blank squares are modifications of the basic types, which are required in almost all applications. If the resonant conditions in a circuit working with soft or resonant switches are broken, the switches will have to cope with hard switching apart from their original features (modified ZVS = MZVS; modified ZCS = MZCS), in order to keep up operation of the whole system (see also chapter 3.8). Mostly, the switches are operated in this deviating mode only for a very short time. In the case of hard active turn-off of a ZVS or hard active turn-on of a ZCS, the switches are operated as ZVHS and ZCHS, respectively.

OFF \ ON	hard	soft L_K in Series	Resonant $i_L = 0$	neutral $V_S = 0$
hard	HS	MZCS		ZVHS
soft C_K in Parallel	MZVS			ZVS
resonant $V_K = 0$				ZVRS
neutral $i_S = 0$	ZCHS	ZCS	ZCRS	NS

Figure 0.13 Power electronic switches

1 Basics

1.1 Application fields and today's application limits of IGBT and MOSFET power modules

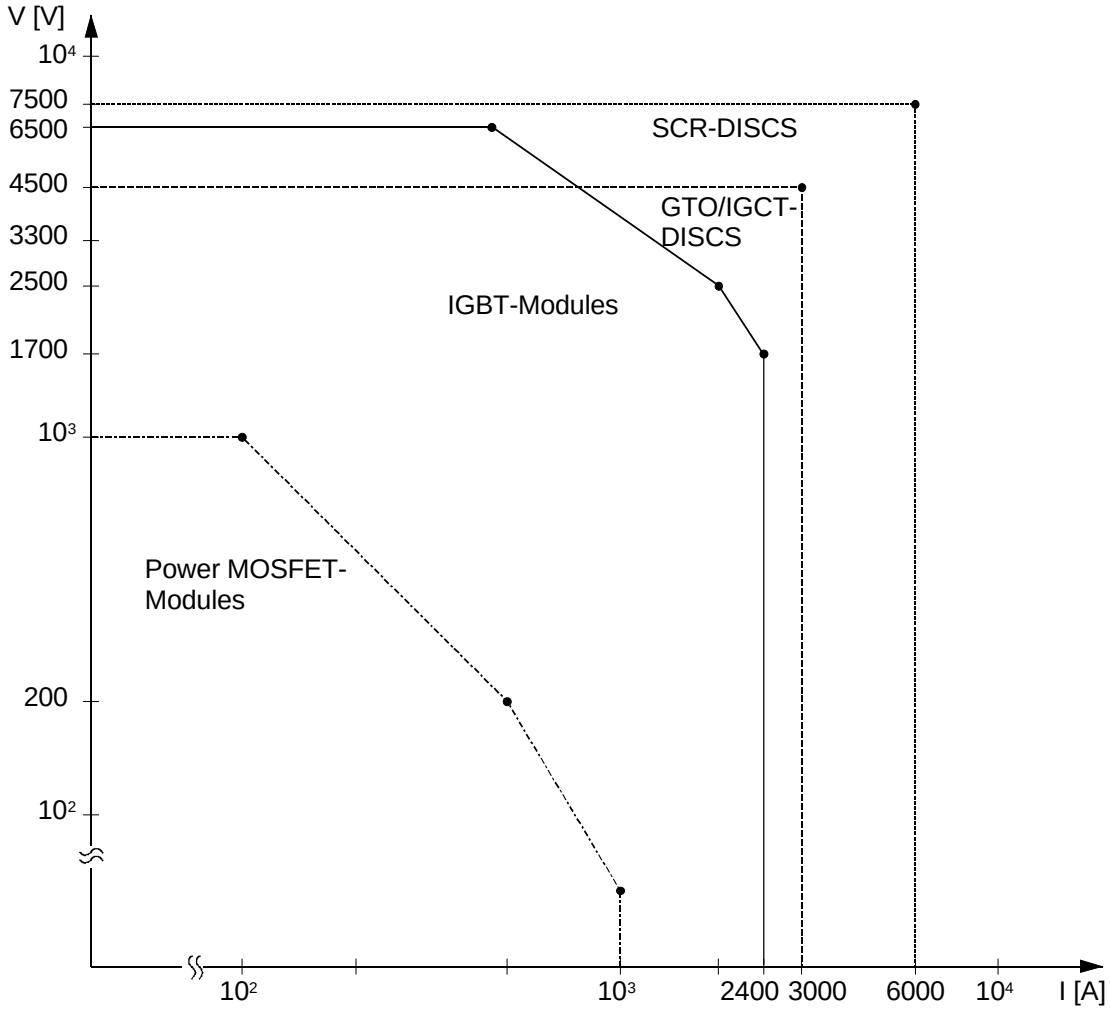


Figure 1.1 Application fields of the latest power semiconductors

As shown in Figure 1.1, a variety of circuitries in power electronics can be produced today with MOSFETs (**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistors) or IGBTs (**I**nsulated **G**ate **B**ipolar **T**ransistors), which were introduced into the market one by one in the mid 80's.
Compared to other switchable power semiconductors, such as conventional GTO-thyristors, these types of transistors have a number of application advantages, such as *active turn-off* even in case of *short-circuit*, operation *without snubbers*, *simple control unit, short switching times* and, therefore, relatively low switching losses.
The production of MOSFETs and IGBTs is comparatively simple and favourable and can easily be managed by today's technologies in microelectronics.
It was mainly due to the rapid development of IGBTs and power MOSFETs that power electronics continued open up new markets, and that their fields of application increased tremendously at the same time. Bipolar high-voltage power transistors that were still very common a few years ago, have been almost completely replaced by IGBTs.

Most applications for currents of some 10A use transistors with silicon chips that are integrated in *potential-free power modules*. These modules contain one or several transistor systems, diodes adapted to the transistors (free-wheeling diodes) and, if required, passive components and „intelligence“, see chapter 1.4..1.6.

Despite the disadvantage of one-side cooling, power modules are maintaining their hold in high-power electronics against the meanwhile also available disc-cells with IGBTs and diodes, which are able to dissipate about 30 % more of the heat losses by two-side cooling. This is mainly due to „integrated“, tested *isolation* of the chips to the heatsink, possible *combinations of different components in one module* and low *costs* due to batch production, apart from their *easy assembly*.

IGBT-modules especially, are going through a permanently successful process of market penetration accompanied by increased efficiency, withstanding the new and further development of other - competitive - power semiconductors. Today IGBT-modules are produced managing a forward blocking voltage of 6.5 kV, 4.5 kV, 3.3 kV and 2.5 kV, e.g. 3.3 kV/2.4 kA [192], [196].
IGBT converters (multi-level-switch and IGBTs in series connection) for the MW-range up to more than 6 kV supply voltage can already be produced now .
MOSFETs, on the other hand, are being developed for even higher frequency applications; also in the high current range more than 500 kHz can be produced with the corresponding wirings and assembly topologies.

Apart from the small power application range, for which chip-on-chip solutions are gaining more and more importance, IGBT and MOSFETmodules are the basic components for the integration of complete electronic and also mechatronic systems in future.

1.2 Power MOSFET and IGBT

1.2.1 Different structures and functional principles

In the following descriptions we restrict ourselves to *n-channel-enhancement power MOSFETs and IGBTs (enhancement transistors)*, representing the majority of transistors used in power modules.
If a *positive control voltage* is applied, a *conducting channel with electrons as charge carriers* (majority carriers) is generated within the existing *p-conducting silicon*. Without applying a control voltage, these components would block (self-blocking).
Other designs, which will not be dealt with any further in this chapter, are *p-channel-enhancement transistors* (induction of a positively charged channel within p-silicon by applying negative control voltage/self-blocking) and *n- and p-channel depletion types (depletion transistors)*, which turn on without applied control voltage (self-conducting). In these transistors, the control voltage generates a space charge zone that cuts off the channel and interrupts the main current flow.
In most applications the *vertical structures* shown in Figure 1.2 and Figure 1.4 are used, where gate and source (MOSFET) or emitter (IGBT) are located on top of the chip, whereas the chip bottom serves as drain (MOSFET) or collector connection. The load current is conducted vertically through the chip outside the channel.
The power MOSFETs and IGBTs shown in the sections have a *planar gate structure*, i.e. a *lateral* (horizontal) conductive channel is generated in case of on-state.
The *planar gate*, which has been further developed to the *double-implanted gate* in modern *high-density* transistors, is the dominating gate structure for power MOSFETs and IGBTs still today.

However, recently developed transistors have a *trench-gate-structure*, with the gates integrated vertically to the structure. During on-state, a *vertical channel* is generated on both sides of the gate. These and other new developments not dealt with any further in this chapter will be discussed in chapter 1.2.4.

The *lateral* MOSFET- and IGBT-structures taken over from microelectronics also have their drain- or collector layer allocated on their chip surface as n+-(MOSFET) or p+-well. Load current is conducted horizontally through the chip. Since the n-zone can be isolated to the IC-substrate by an oxide layer, several isolated MOSFETs or IGBTs may be integrated together with other structures on one chip.
Due to the fact that lateral transistors are only able to generate a current density of about 30 % of that in vertical structures and, thus, require more space on the assembly, they are used preferably in complex, monolithic circuits.

The structural design of the power MOSFET (Figure 1.2) as well as the IGBT (Figure 1.4) consists of a silicon-micro-cellular structure of up to 820,000 cells per cm^2 (latest high-tech 60 V-MOSFETs) or about 100,000 cells per cm^2 (high-voltage-IGBTs) distributed over a chip surface of 0.3...1.5 cm^2.

The cell-sections show the analogue structure of the MOSFET and IGBT control zones.
The n^--zone has to take up the space charge zone during off-state and accommodates p-charged wells with a low marginal (p^-) and a high central (p^+) doping.
These wells also include n^+-silicon-layers which are connected to the aluminium- metallized source (MOSFET) or emitter (IGBT) electrode. A control zone (gate) consisting, for example, of n^+-polysilicon is embedded in a thin isolation layer of SiO_2 above the n^+-areas.

By applying a sufficient positive control voltage between gate and source (MOSFET) or emitter (IGBT), an inversion layer (n-conducting channel) is generated in the p-area below the gate. Electrons may be conducted from source or emitter to the n^--drift-area via this channel.
In contrast to the identical structure of MOSFET and IGBT including the n^--zone, there are differences regarding the third electrode, which will determine all further functions.

Power-MOSFET [277]

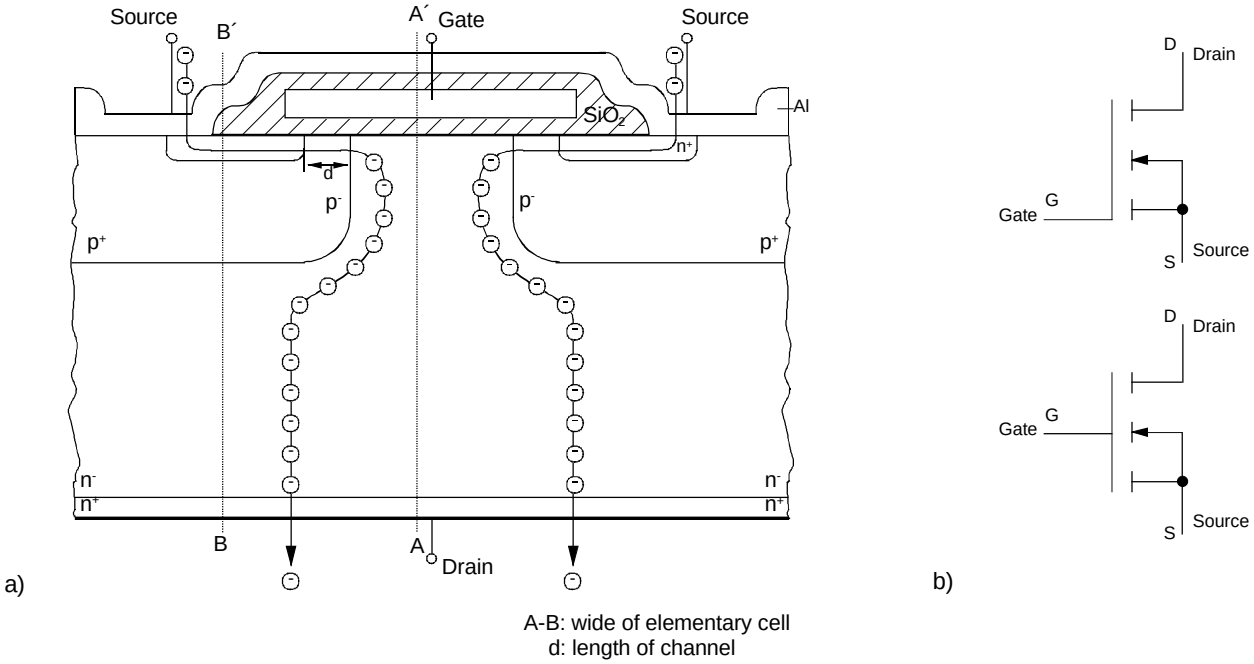


Figure 1.2 Power-MOSFET (SIPMOS Siemens)
a) MOSFET-cell with charge flow during on-state
b) Common switch symbols

Figure 1.2 explains the structure and function of a *vertical n-channel-enhancement* power-MOSFET with *planar* gate structure.

The MOSFET's layer structure described above results from epitaxial, implantation and diffusion processes on a substrate of n^+-conductive silicon material with a drain contact on its reverse side.
The electrons flowing in the electrical voltage field between drain and source are attracted by the drain connection, thus absorbing the space charge zone; consequently, the drain-source voltage will decrease and the main current (drain current) will be able to flow.
Since the electrons are conducting current by 100 % and are majority charge carriers in the n^--drift area, the highly resistive n^--zone will not be flooded by bipolar charge carriers; the MOSFET is a *unipolar* component.
Whereas the drain-source on-resistance of low-voltage MOSFETs is composed of single cellular resistances about 5 % to 30 %, 95 % of the $R_{DS(on)}$ of high reverse voltage MOSFETs result from the n^--epitaxial area resistance.
Therefore, on-state voltage drop

$V_{DS(on)} = I_D \cdot R_{DS(on)}$ with I_D: drain current and

$R_{DS(on)} = k \cdot V_{(BR)DS}^{2.4...2.6}$ with k: material constant, e.g. $k = 8.3 \cdot 10^{-9}\ A^{-1}$ for a chip surface of 1 cm^2;

$V_{(BR)DS}$: Drain-source forward breakdown voltage

as a theoretical limit value of the actually available MOSFETs is always higher for MOSFETs from about 200...400 V off-state voltage than for comparable bipolar components and the current

carrying capacity is lower. Recently developed structures with improved parameters will be dealt with in chapter 1.2.4.
On the other hand, there are no storage effects because the majority charge carriers are exclusively responsible for charge transportation. Very short switching times may be produced however, requiring rather high control currents for changing the internal capacitances in the case of extensive components (high voltage/ high current) with about 0.3 µC per cm^2 chip surface.
The capacitances resulting from the physical structure of the MOSFETs are the most important parasitic elements in Figure 1.3; their influence on the characteristics of components will be described in the corresponding chapters.

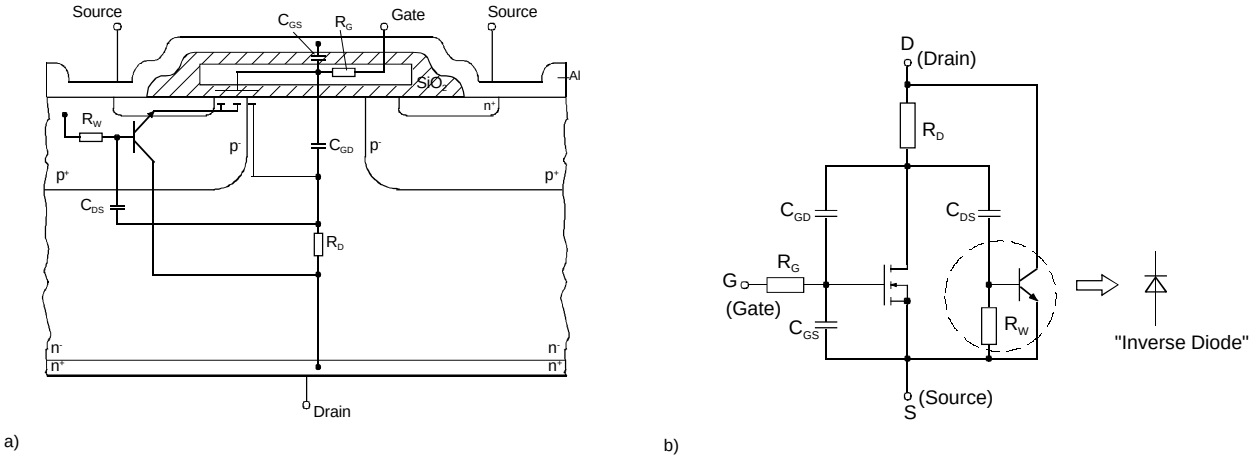


Figure 1.3 Power-MOSFET-cell with the most important parasitic elements
a) Parasitic elements within the cellular structure
b) Equivalent circuit with parasitic elements

The follwing table explains causes and designations of the parasitic capacitances and resistances in Figure 1.3:

Symbol	**Designation**	
C_{GS}	Gate-source capacitance	Overlapping gate and source metallization; dependent on gate-source voltage; independent of drain-source voltage
C_{DS}	Drain-source capacitance	Junction capacitance between n^--drift zone and p-well; dependent on cell surface, drain-source breakdown voltage and drain-source voltage
G_{GD}	Gate-drain capacitance	Miller capacitance; generated by overlapping of gate and n^--drift zone
R_G	Gate resistance (internal)	Poly-silicon-gate resistance; in modules with several transistor chips often additional series resistors are needed to minimize oscillations between chips
R_D	Drain resistance	Resistance of n^--zone; often main part of MOSFET-*on-state-resistance*
R_W	Lateral resistance of p-well	Base-emitter resistance of parasitic npn- bipolar transistor

IGBT [278]

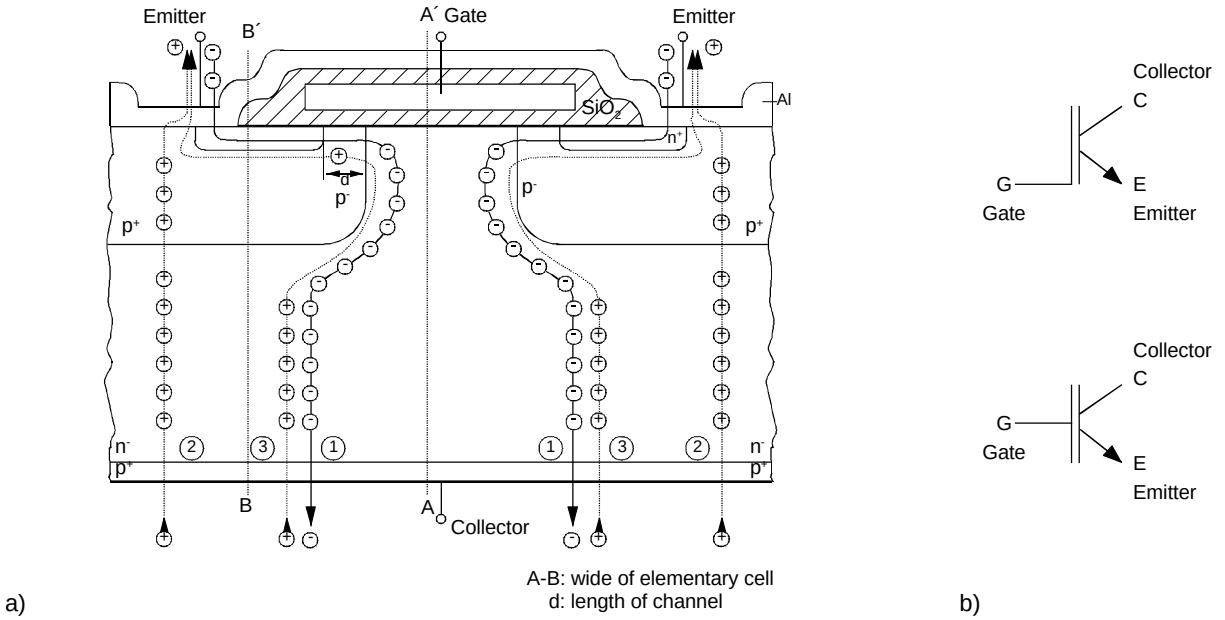


Figure 1.4 IGBT with NPT-structure
a) IGBT-cell with charge distribution during on-state
b) Common switch symbols

Figure 1.4 explains structure and function of a *vertical n-channel-enhancement* IGBT with *planar* gate and NPT-*(**N**on-**P**unch-**T**hrough)-structure.*

In contrast to MOSFETs, IGBTs are equipped with a p^+-conductive area with connection to the collector below the n-zone.
After having passed the n^--drift area, the electrons enter the p^+-area, thus arranging for positive charge carriers (holes) to be injected from the p+-zone to the n^--zone. The injected holes will flow directly from the drift-area to the emitter-p-contact as well as laterally to the emitter passing the MOS-channel and the n-well. In this way the n^--drift area will be flooded with charge carriers which are conducting the main current (collector current); this charge enhancement will lead to a space charge reduction and, consequently, to a reduction of the collector-emitter voltage.

Although, compared to the pure ohmic on-state behaviour of the MOSFET, the IGBT has an additional threshold voltage at the collector pn-junction layer, the on-state voltage of high-voltage IGBTs (from about 400V) is lower than that of MOSFETs because of the enhancement of minority carriers in the highly resistive n^--zone. In comparison to MOSFETs, IGBTs may be designed for considerably higher voltages and currents for similar chip surfaces.
On the other hand, the surplus p-storage charge Q_S that has not been extracted during the collector voltage increase period has to recombine in the n^--zone during turn-off. Q_s has an almost linear characteristic in the low-current range and rises proportionally to the forward current in the rated current and overcurrent range according to a radical law. [282]:

$Q_s \sim I^{0.8...1}$ in the low-load forward current range
$Q_s \sim I^{0.5}$ in the rated current and overcurrent range.
$Q_s \sim V_{(BR)CE}^{2...2.7}$

Storage charge enhancement and depletion processes cause switching losses, a delay time (storage time) and a collector tail-current during turn-off. (see chapter 1.2.3).

Apart from the "**N**on-**P**unch-**T**hrough"-structure (NPT) shown in Figure 1.3, the "**P**unch-**T**hrough" (PT)-structure is also applied in IGBTs today. It was the conceptional basis for the first IGBTs.
Basically, the two structures differ in the PT-IGBT's highly-doped n^+-layer (buffer layer) between n^-- and p^+-zone and in the manufacturing process.
Whereas the n^+- and n^--layers in a PT-IGBT are usually generated on a p^+-substrate by an epitaxial procedure, the basis of the NPT-IGBT is a thin, hardly doped n-wafer, at the reverse side of which the collector p+-zone is generated by implantation. The MOS-control zones on top of both IGBTs are identical in their planar structure.

Figure 1.5 compares both IGBT-structures and their electrical field characteristics during off-state.

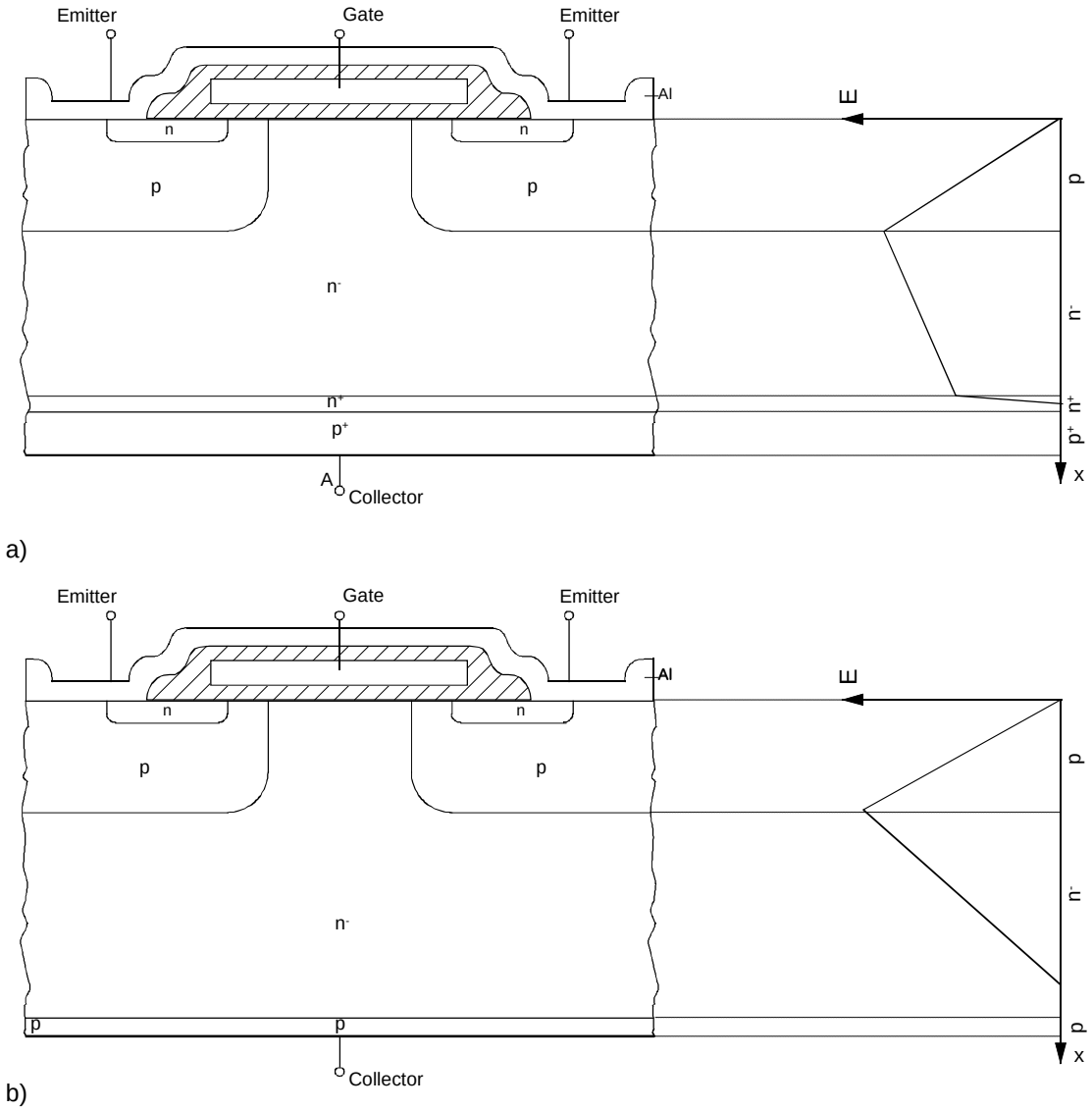


Figure 1.5 IGBT-structures and off-state electrical field characteristics [193]
a) PT-IGBT
b) NPT-IGBT

The space charge zone in a *PT-IGBT* or *IG**E**T* (**E**: **e**pitaxial structure) spreads over the whole n^--area during off-state. In order to keep the epitaxial layer as thin as possible for high off-state voltages also, the electrical field is reduced by the highly doped n^+-buffer at the end of the n^--drift area.
The n^--drift area in an *NPT-IGBT* or *IG**H**T* (**H**: **h**omogeneous structure) is dimensioned large enough so that the electrical field can be completely discharged within the n^--drift area during off-state at maximum off-state voltage. The electrical field cannot spread over the whole n^--zone (punch through) within the permissible operation range.

For further explanations on IGBT-functions and the deviating characteristics of PT- and NPT-components it is, first of all, necessary to study the equivalent circuit resulting from the IGBT-structure (Figure 1.6b).

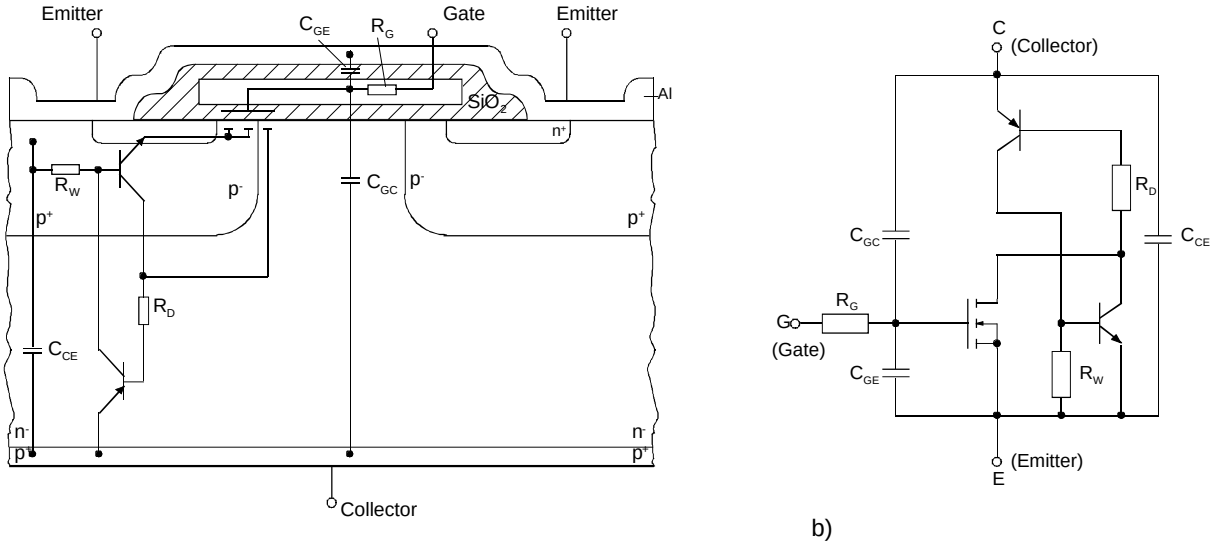


Figure 1.6 IGBT-cell (NPT-structure) with the most important parasitic elements
a) Parasitic elements in the cellular structure
b) Equivalent circuit with parasitic elements

Causes and designations of the parasitic capacitances and resistances in Figure 1.6 are analogous to Figure 1.3.

Symbol	**Designation**	
C_{GE}	Gate-emitter capacitance	Overlapping gate and source metallization; dependent on gate-emitter voltage; independent of collector-emitter voltage
C_{CE}	Collector-emitter capacitance	Junction capacitance between n^--drift zone and p-well; dependent on cell surface, drain-source breakdown voltage and drain-source voltage
G_{GC}	Gate-collector capacitance	Miller-capacitance: generated by overlapping of gate and n^--drift zone
R_G	Gate resistance (internal)	Poly-silicon-gate resistance; in modules with several transistor chips often additional series resistors are needed to minimize oscillations between chips
R_D	Drift resistance	Resistance of n^--zone (base resistance of a pnp-transistor)

Symbol	Designation	
R_W	Lateral resistance of p-well	Base-emitter resistance of the parasitic npn-bipolar transistor

Apart from internal capacitances and resistances, the equivalent circuit of the IGBT also shows features of the „ideal MOSFET“ and the parasistic npn-transistor: n^+-emitter zone (emitter)/p^+-well (base)/n-drift zone (collector) with the lateral p^+-well resistance below the emitters as base-emitter resistance R_W. In addition to that a pnp-transistor may be generated by sequence of p^+-collector (emitter)/ n^--drift (base)/ p^+-well (collector), which represents together with the npn-transistor thyristor circuit.
Latch-up of this parasitic thyristor may happen basically during on-state (when a critical current density is exceeded, which decreases with rising chip temperature) and also during turn-off (dynamic latch-up due to the increased hole current compared to on-state operation), as soon as the following latch-up preconditions are met:

$$M \cdot (\alpha_{npn} + \alpha_{pnp}) = 1 \qquad \text{with} \quad \alpha_{pnp}, \alpha_{npn} = \alpha_T \cdot \gamma_E$$

M: multiplication factor;
α_{npn}, α_{pnp}: current gain of the single transistors in base circuit;
α_T: base transportation factor;
γ_E: emitter efficiency

This will lead to a loss of controllability of the IGBT and, therefore, to its destruction.

The following design measures will reliably prevent latch-up in modern IGBTs under all permissible static and dynamic operation conditions; the turn-off current density of dynamic latch-up, for example, is about 15 times the rated current density.
At first, the base-emitter resistance R_W of the npn-transistor is reduced by means of
- high doping of the p^+-well directly below the n-emitters, and
- shortening of the n-emitters

to such an extent, that the threshold voltage of the npn-transistor base-emitter diode will not be reached in any permissible state of operation.
Furthermore, the hole current (npn-transistor base current) is kept on a minimum level by a low current amplification in the pnp-transistor. However, switching behaviour and ruggedness have to be optimized with the on-state characteristics which also depend considerably on the pnp-transistor design.
This has been produced for PT- and NPT-IGBTs in different ways [278].

For *PT-IGBTs*, the efficiency (emitter efficiency) of hole injection of the p^+-zone into the n^--drift area is very high, since the substrate is very thick and highly doped. The pnp-current amplification may only be lowered with the help of the base transportation factor (n^--drift zone, n^+-buffer), implementing additional recombination centres (e.g. by gold doping or electron beam radiation) to reduce charge carrier life time in the n^+-zone.
The hole current adds up to 40...45 % of the total current.
In case of *NPT-IGBTs* the p+-emitter zone generated at the collector by implantation is much thinner than the PT-IGBT-substrate. Therefore, the doping material concentration can be exactly dimensioned during wafer production. The very thin p+-layer guarantees a low emitter efficiency (γ_E = 0,5) of the pnp-transistor, so that it is not necessary to lower the base transportation factor by reducing charge carrier life time.
The hole current sums up to 20...25 % of the total current.

Compared to the PT-IGBT, the NPT-IGBT shows the following advantages resulting from diminished emitter efficiency, longer charge carrier life time and more exact design possibilities, which is still to be detailed in chapters 2 and 3:

- positive on-state voltage temperature coefficient (”automatic” static balancing in the case of parallel connection),
- lower, but partly longer turn-off tail current; lower turn-off losses at $T_j = 125°C$,
- (in the case of hard switching) shorter switching times and reduced switching losses,
- considerably reduced temperature dependency of switching times / switching losses ($T_j = 125°C$) and tail current,
- increased overcurrent stability by improved current limitation in case of overload.

Compared to the epitaxial substrates of the PT-IGBT, today’s production of the homogeneous n^--substrate as basic material for NPT-IGBTs is more favourable, provided that the much thinner silicon wafers are handled properly.

1.2.2 Static behaviour

In this chapter the static behaviour of power MOSFETs- and IGBT-modules is to be examined regarding the current-voltage characteristics of the main terminals in the I^{st} and III^{rd} quadrant of the respective output characteristic (Figure 1.7).

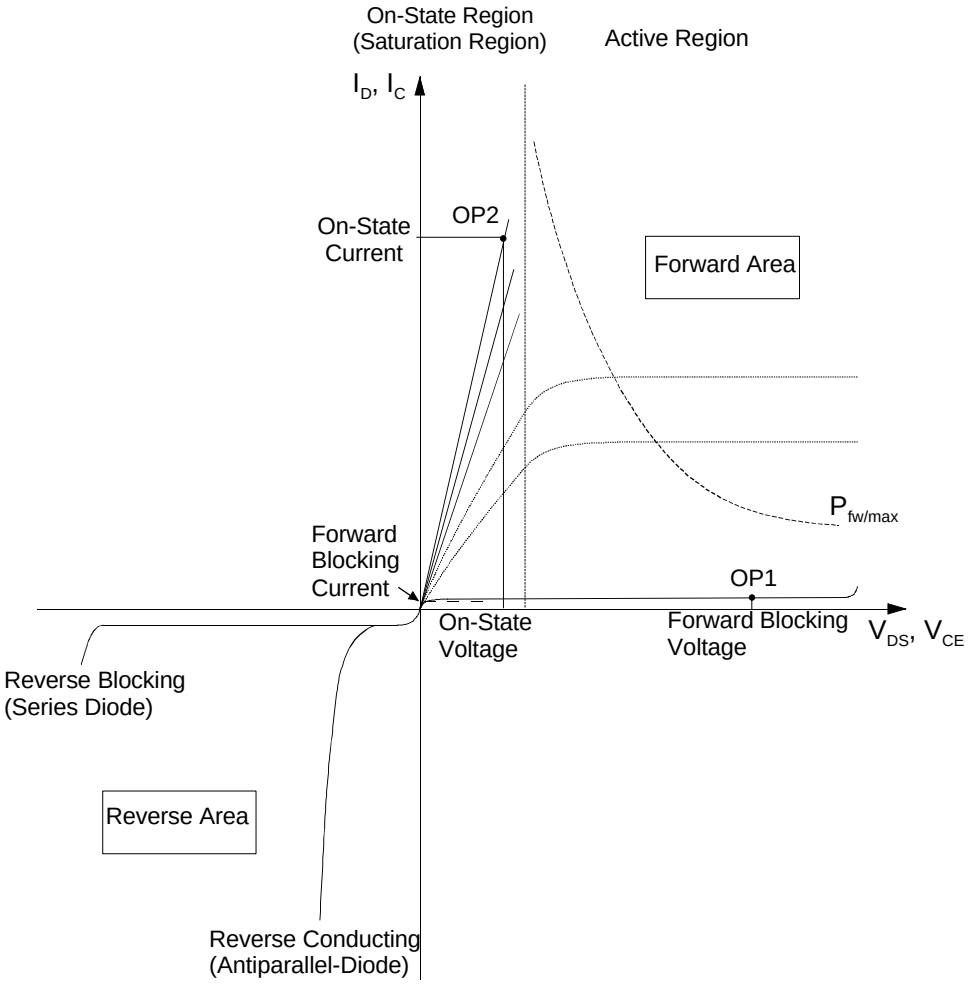


Figure 1.7 Basic output characteristic of a power transistor module

The Ist quadrant shows the *forward area*, where power transistor modules can block high voltages and switch high currents.

The exact designation "*blocking state*" - analogous to thyristors - for blocking in the Ist quadrant is hardly used in connection with transistors. Usually, this is called „*forward off- state*" (as in the following explanations) or „*off-state"* (as long as there is no risk of confusion).

Via the gate electrode, the power-MOSFET or IGBT is turned from the *forward off- state* (OP1 in Figure 1.7) to the *conductive state* or *on-state* (OP2), where it can conduct load current. The *active* region is only passed during switching.
Contrary to the „perfect switch" off-state voltage and on-state current are limited (see chapter 0). During the forward off-state a cut-off current (*forward off-state current*) causes blocking power dissipation within the transistors.

In the conductive state the voltage left at the main power terminals depends on the on-state current and is called *on-state voltage*, causing on-state power dissipation. The maximum power dissipation during on-state (not during switching) is shown by the on-state power dissipation hyperbola for $P_{fw/max}$ in the output charcteristic.

The current-voltage characteristics in the IIIrd quadrant of the output characteristic show the *reverse* behaviour of power transistor modules, in case a negative voltage is applied to the main terminals. This behaviour is determined by the characteristics of the transistors (reverse blocking, reverse conducting) and the features of the diodes within the power module (connected in series or anti-parallel to the transistors).

1.2.2.1 Power-MOSFET

The functional principles of the power-MOSFET described above result in the output characteristics in Figure 1.8a.

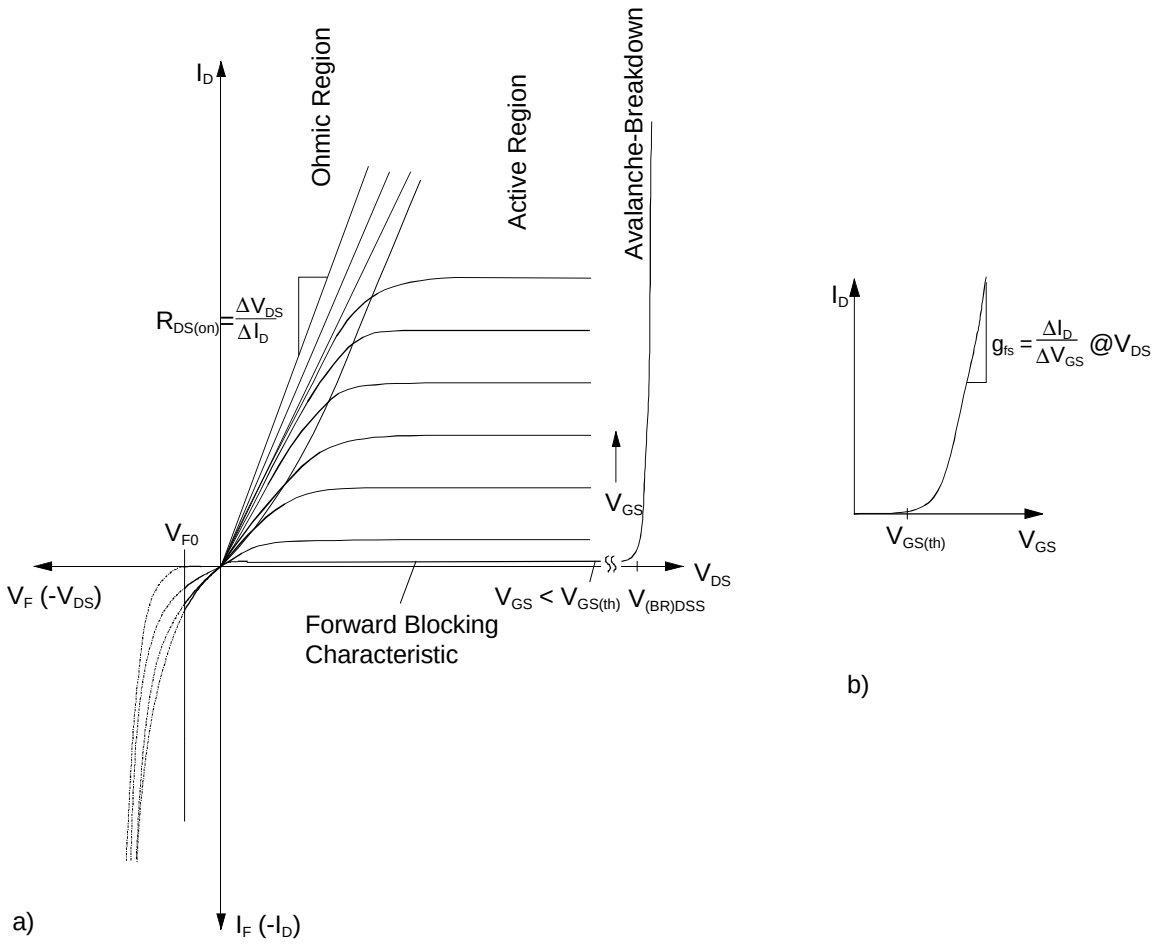


Figure 1.8 a) Output characteristics of a power-MOSFET (n-channel-enhancement-type)
b) Transfer characteristic $I_D = f(V_{GS})$

Forward off-state

When applying a positive drain-source voltage V_{DS} and a gate-source voltage V_{GS} smaller than the gate-source threshold-voltage $V_{GS(th)}$, there will only be a very small zero gate voltage drain current I_{DSS} between drain- and source connection.

I_{DSS} will rise slightly with increasing V_{DS}. If a certain specified maximum drain-source voltage V_{DSS} is exceeded, this will cause an avalanche breakdown of the pin-junction p^+-well/n^--drift zone/n^+-epitaxial layer (breakdown voltage $V_{(BR)DSS}$). Physically, $V_{(BR)DSS}$ is almost equivalent to the breakdown voltage V_{CER} of the parasitic bipolar npn-transistor in a MOSFET, generated by the sequence of layers: n^+-source zone (emitter)/p^+-well (base)/n^--drift zone/n^+-epitaxial layer-drain connection (collector), see Figure 1.3.
The multiplication current generated by the avalanche breakdown of the collector-base diode may lead to destruction of the MOSFET as soon as the bipolar transistor is turned on.
However, the base and emitter zones are almost short-circuited by metallization of the source; both zones are only separated by the lateral resistance of the p^+-well.
Several structural improvements, such as small MOSFET cells, homogeneous cell arrangement, low-resistive p+-wells, optimized marginal structures and highly homogeneous technological procedures, may facilitate a very small avalanche breakdown current per cell in modern MOSFETs, so that the bipolar transistor will not yet be turned on, in case the defined specifications are strictly complied with.

Therefore, a permissible avalanche energy E_A for single pulses or periodic load (limited by the maximum chip temperature) can be defined; see chapter 2.2.1.
Since several parallelled MOSFET-chips in power modules cannot guarantee absolute symmetrical conditions, the maximum E_A-value is only applicable for one single chip.

On-state

The forward on-state at positive drain-source voltage V_{DS} and positive drain current I_D can be divided into two characteristic regions (Figure 1.8, I[st] quadrant).

Pinch-off or active region

At a gate-source voltage V_{GS} slightly exceeding the threshold voltage $V_{GS(th)}$, current saturation will cause a considerable drop of voltage over the channel (horizontal region of the output characteristic). The drain current I_D is controlled by V_{GS}.
The transfer behaviour shown in Figure 1.8b is called *forward transconductance* g_{fs} defined as follows:

$g_{fs} = dI_D/dV_{GS} = I_D/(V_{GS}-V_{GS(th)})$.

Forward transconductance in the pinch-off region rises proportionally to the drain current I_D and the drain-source-voltage V_{DS} and drops with increasing chip temperatures.
Within the permissible operation conditions for power modules with several paralleled MOSFET-chips, the pinch-off region is only passed during turn-on and turn-off.
On the other hand, stationary operation within the pinch-off region is mostly prohibited by the manufacturer, because $V_{GS(th)}$ will drop when the temperature rises and, therefore, thermal instability between the single chips might result from minor production deviations.

Ohmic region

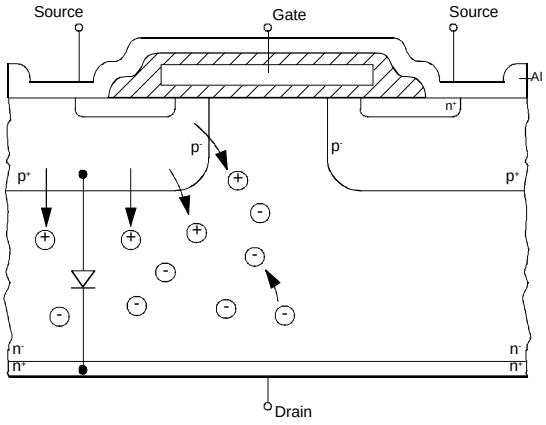
The ohmic region, which is also called on-state during switching operations, is reached as soon as I_D is determined only by the outer circuit. The on-state behaviour can be characterized as the quotient of changed drain-source-voltage V_{DS} and drain-current I_D via the turn-on resistance $R_{DS(on)}$. Consequently, the forward voltage $V_{DS(on)}$ may be defined by the following equation already mentioned in chapter 1.2.1 (large-signal behaviour)

$$V_{DS(on)} = R_{DS(on)} \cdot I_D$$

$R_{DS(on)}$ is dependent on the gate-source voltage V_{GS} and the chip temperature. $R_{DS(on)}$ is approximately doubled within the MOSFET operation temperature range between 25°C and

Reverse operation

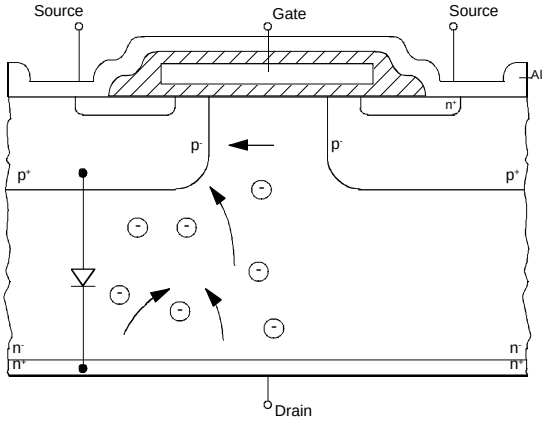
During reverse operation (III[rd] quadrant) the MOSFETcharacteristic is equivalent to a diode characteristic at $V_{GS} < V_{GS(th)}$ (continuous curve in Figure 1.8a). This is caused by the parasitic diode within the MOSFET; the MOSFET reverse on-state behaviour at closed channel is controlled by the on-state voltage of the collector-base pn-junction or source-drain pn-junction, respectively („inverse diode“, *bipolar current flow*) (Figure 1.9a).



V_{GS} = 0 V

V_{DS} = $-V_F$

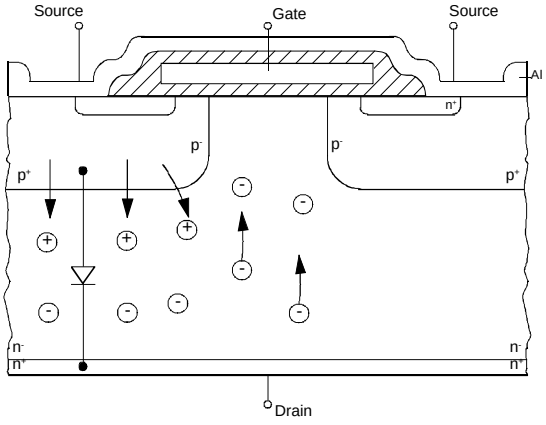
a)



$V_{GS} > V_{GS(th)}$

$V_{DS} > -V_{F0}$ (z.B. -0.2 V)

b)



$V_{GS} > V_{GS(th)}$

$V_{DS} < -V_{F0}$ (z.B. -0.7 V)

c)

Figure 1.9 Inverse operation of a power-MOSFET [277]
a) At closed channel (bipolar current flow)
b) At open channel and small negative V_{DS} (unipolar current flow)
c) At open channel and big negative V_{DS} (combined current flow)

The bipolar inverse diode is utilized for currents up to the limit values specified for MOSFETs. In practice, however, the inverse diode

- causes relatively high on-state power losses, which have to be dissipated together with the MOSFET power losses and

- sets limits to the MOSFET's application field as a „hard switch" (see chapter 0) by its unfavourable turn-off behaviour.

As shown in Figure 1.9b the conductance in the MOSFET-channel is principally controllable even at a negative drain-source-voltage, if a gate-source voltage is applied exceeding the threshold voltage.
If the drain-source voltage is limited to a value lower than the inverse diode threshold voltage by external components, for example by paralleling of a Schottky-diode, the inverse current will be conducted from drain to source as a *unipolar electron current* (majority carrier current). Then, the turning-off corresponds to the turn-off behaviour of a MOSFET.
The inverse current is dependent on V_{DS} and V_{GS}. (broken curve in Figure 1.8a).

Operation with *combined current flow* according to Figure 1.9c (semi-coloned curve in Figure 1.8a) is given, if the channel is open and a conducting bipolar inverse diode is connected (drain-source voltage higher than diode threshold voltage). This results in a reduced on-state voltage compared to simple paralleling of diode and MOSFET, since the injected charge carriers will also diffuse laterally, thus increasing the MOSFET's conductivity.

Apart from that, MOSFET-chips with fast inverse diodes have been developed by several manufacturers during the past few years (e.g. FREDFETs; **F**ast **R**ecovery **E**pitaxial **D**iode **F**ield **E**ffect **T**ransistors)[277]. Hole life time at inverse operation is minimized in FREDFET-chips by selective heavy-metal diffusion into the n^--drift area, similar to the design of fast diodes.

1.2.2.2 IGBT

The functional principle of the IGBT described in chapter 1.2.1 results in the output characteristic in Figure 1.10.

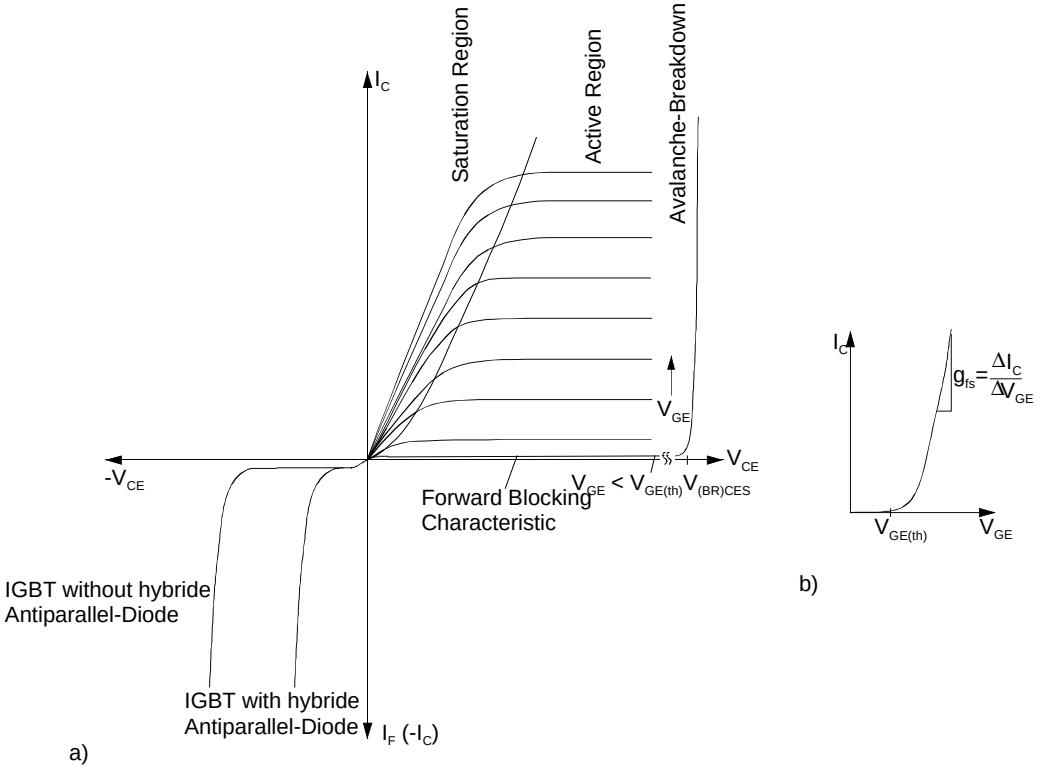


Figure 1.10 a) Output characteristic of an IGBT (n-channel-enhancement-type)
b) Transfer characteristic $I_C = f(V_{GE})$

Forward off-state

In analogy to the MOSFET, the collector-emitter cut-off current I_{CES} between collector and emitter is only very small, if the collector-emitter voltage V_{CE} is positive and the gate-emitter voltage V_{GE} is lower than the gate-emitter threshold voltage $V_{GE(th)}$.
As a consequence of increasing V_{CE}, the I_{CES}-value rises slightly. When a certain specified maximum collector-emitter voltage V_{CES} is exceeded, there will follow an avalanche breakdown of the pin-junction layers p^+-well/n^--drift zone/n^+-epitaxial layer (avalanche breakdown voltage $V_{(BR)CES}$). Physically, $V_{(BR)CES}$ corresponds approximately to the reverse collector-emitter voltage V_{CER} of the *bipolar pnp-transistor* in the IGBT structure. (see Figure 1.6).
The multiplication current generated by the avalanche breakdown of the collector-base diode may lead to destruction of the IGBT, as soon as the bipolar transistor is turned on.
However, base and emitter are almost short-circuited by metallization of the emitter, only separated by the lateral resistance of the p^+-well.
By several structural improvements within the IGBT, similar to the measures taken for MOSFETs as described in chapter 1.2.2.1, the avalanche breakdown current per cell is kept at a minimum level, which results in a high forward off-state voltage stability (avalanche stability).

On-state

Also with the IGBT, the forward on-state at a positive collector-emitter voltage V_{CE} and a positive collector current I_C can subdivided up in two characteristic regions (Figure 1.10, I^{st} quadrant).

Active region

At a gate-emitter voltage V_{GE} slightly exceeding the threshold voltage $V_{GE(th)}$, current saturation will cause a considerable voltage drop over the channel (horizontal region of the output characteristics). The collector current I_C is controlled by V_{GE}.
The transfer behaviour shown in Figure 1.10b is called - in analogy to the MOSFET - *forward transconductance* g_{fs} defined as follows:

$$g_{fs} = dI_C/dV_{GE} = I_C/(V_{GE}-V_{GE(th)})$$

Forward transconductance in the cut-off region rises proportionally to the collector current I_C and the collector-emitter voltage V_{CE}, and decreases with increasing chip temperatures.
Within the permissible operation conditions for power modules with several paralleled IGBT-chips, the cut-off region is only passed during turn-on and turn-off.
Equivalent to MOSFET modules, stationary operation within the cut-off region will mostly be prohibited, since $V_{GE(th)}$ will decrease when the temperature rises and, also with IGBTs, thermal instability between the single chips might result from minor production deviations.

Saturation region

The saturation region (steep region of the output characteristic), also called on-state during switching operation, is reached as soon as I_C is determined only by the outer circuit. The on-state behaviour is characterized by the IGBT voltage V_{CEsat} (collector-emitter saturation voltage). At least for highly blocking IGBTs, the saturation voltage is considerably smaller than the on-state voltage of a comparable MOSFET due to the n^--drift-zone being flooded with minority carriers.
As already mentioned, V_{CEsat} of PT-IGBTs will drop at a temperature increase within rated current operation, whereas V_{CEsat} of NPT-IGBTs will rise proportionally to the temperature.

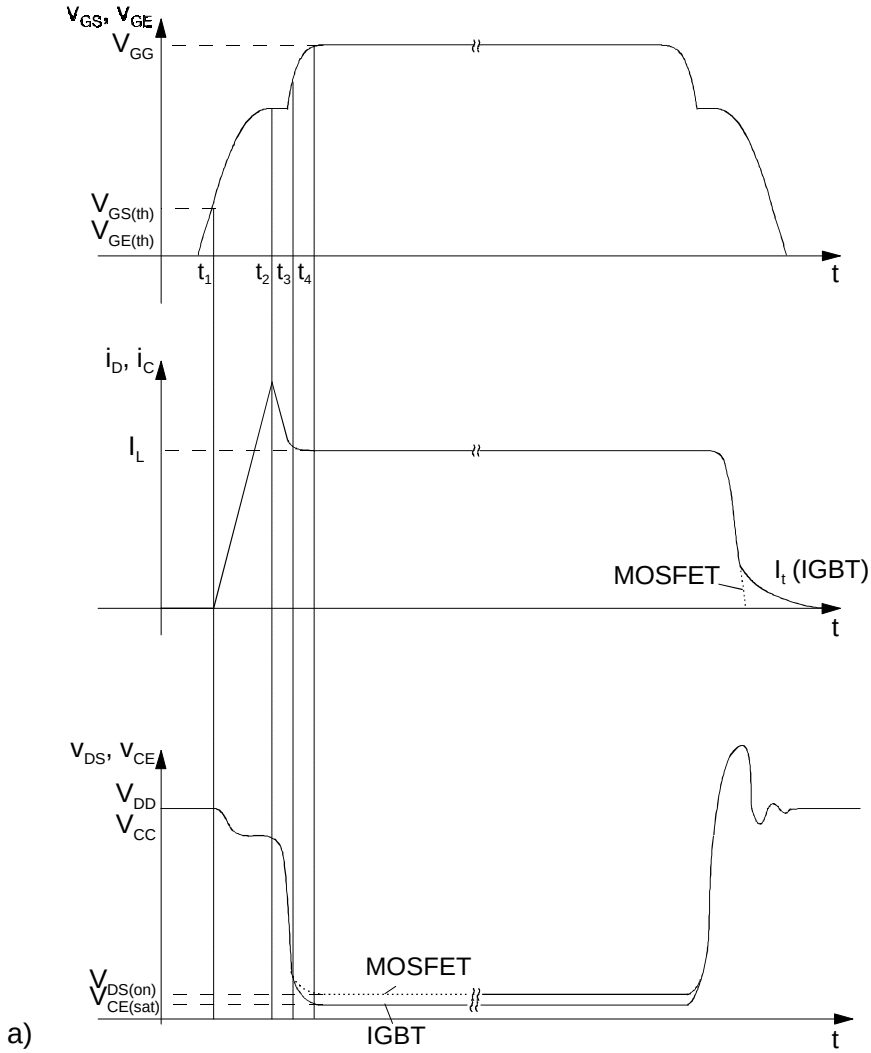
Reverse operation

During reverse operation (Figure 1.10, IIIrd quadrant) the IGBT collector pn-junction is poled in reverse direction and there is no inverse conductivity, other than with MOSFETs.
Although, due to the large n$^-$-drift zone, this is actually the structure of a highly resistive pin-diode, at least in the case of NPT-IGBTs, the reverse voltage in today's IGBTs is only some 10V. Apart from design of the chip margin, this is due to the fact that the chips have been designed mainly to comply with a high off-state voltage and an optimized collector heat dissipation.
IGBT-switches designed for special reverse applications have therefore been equipped solely with adapted, fast hybrid diodes connected in series.

So, the characteristics of the external or hybrid diodes (see chapter 1.3) are exclusively responsible for the reverse on-state behaviour of IGBT-modules.

1.2.3 Hard switching behaviour of MOSFETs and IGBTs

Most switching applications for transistor switches require „hard" switching of ohmic-inductive loads with continuous load current, i.e. the time constant of the load L/R is much bigger than the cycle l/f of the switching frequency.
The resulting basic waveforms for drain or collector current and drain-source or collector-emitter voltage are shown in Figure 1.11a.



a)

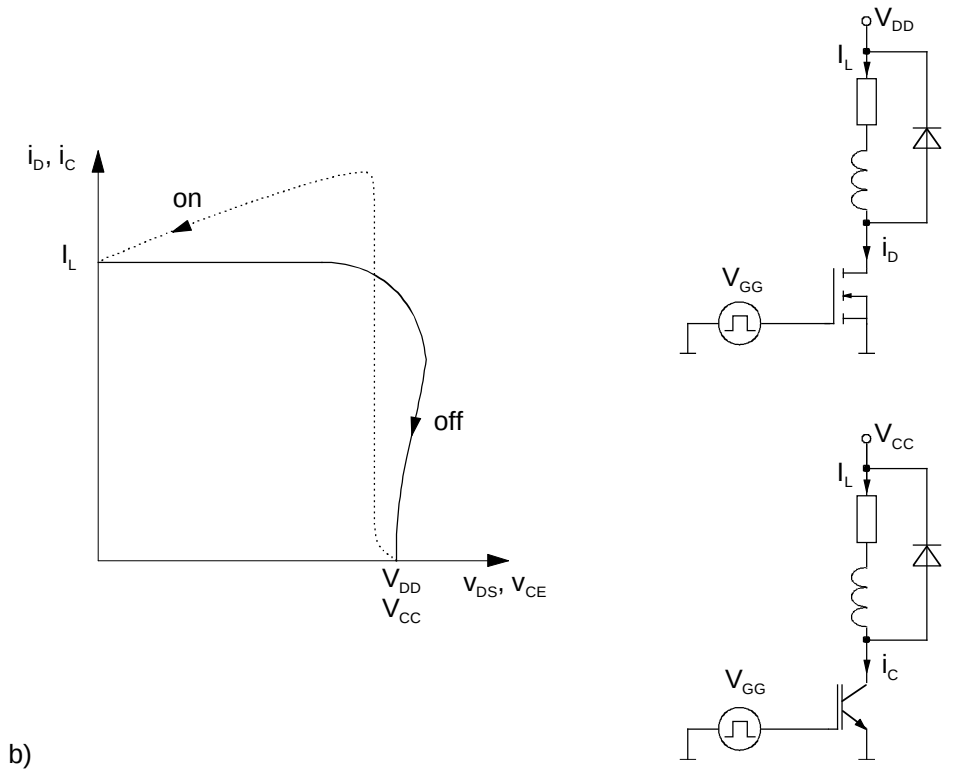


Figure 1.11 Typical "hard" switching behaviour of MOSFET and IGBT (ohmic-inductive load with free-wheeling circuit)
a) Current and voltage waveforms
b) Curve and measurement circuit

As already depicted in chapter 0, Figure 0.4 a high short-time transistor current and voltage during turn-on and turn-off are typical features of „hard switching".
In contrast to all types of thyristors, such transistors operate without passive snubber networks thanks to the „dynamic" junction which is generated in the drift zone during switching operation. In a transistor, however, considerable switching energy

$$E_{on}, E_{off} = \int_{t_{on}, t_{off}} u \cdot i dt$$

is dissipated as explained by the graph $i_C = f(v_{CE})$ (and $i_D = f(v_{DS})$) in Figure 1.11b.
The curve may be directed nearer towards the axes with passive snubber networks. Switching losses are „shifted" from the transistor to the snubber, the total efficiency will decrease in most cases (chapter 3.8).
Since the size of the operating area is influenced by many (non-ideal) transistor features apart from current/ voltage limitations and switching times, the SOA (**S**afe **O**perating **A**rea) is given in the datasheets for different operating conditions (see chapters 2.1.2, 2.2.3 and 2.3.3).
Moreover, passive circuit elements have a tremendous influence on switching losses and operating areas, apart from the non-ideal transistor features and the diode characteristics described in chapter 1.3. The effects of such passive circuit elements also indicated in Figure 1.11a are explained in detail in chapter 3.4.1.

Physically, the typical current-voltage characteristics in Figure 1.11a are caused by the free-wheeling diode, which has to prevent current snap-off by load inductance:

- When the transistor is turned on, the free-wheeling diode can only take up reverse recovery voltage (turn off), after the load current has completely commutated to the transistor. Therefore, the collector or drain-current has to reach the load current level, before the collector-emitter (or drain-source) voltage may fall to the on-state value.
- When the transistor is turned off, the free-wheeling diode can only take up the load current (turn on), after it has reached on-state voltage polarity. This will be the case when the collector-emitter (or drain-source) voltage has exceeded the commutation voltage level, before the collector or drain-current may fall to the cut-off current value.

As shown in Figure 1.11a, the drain-source or collector-emitter voltage of comparable components will, shortly after *turn-on* of the MOSFET or IGBT, drop within some 10ns to a value, that is equivalent to the voltage drop over the n^--drift area. Whereas in the MOSFET the on-state voltage has already been reached by this, the n^--area of the IGBT is now flooded with positive charge carriers from the p-collector zone. After this procedure has been finished (appr. 100ns up to some µs), the static value of the on-state saturation voltage $V_{CE(sat)}$, which is relatively low for highly blocking components, has been reached (conductivity modulation).

During *turn-off* of the MOSFET, the internal capacitances have to be recharged, that there are no charge carrier influence left in the channel area. Thereafter, the neutrality interferences in this area will quickly be reduced and the drain current will drop rapidly.
The procedure within the IGBT is principally the same. However, after the emitter current in the n^--drift zone has been turned off, a large number of p-charge carriers generated by injection from the IGBT-collector zone is still left. These p-charge carriers have now to be recombined or reduced by re-injection, which would cause a so-called collector tail current I_t. (Figure 1.11a).
Since this tail current will fade away within some µs only with already increased collector-emitter voltage, the hard turn-off power losses in the IGBT are mainly determined by the tail current waveform (see chapter 2.3.2, 3.1.3) and are considerably higher than those in MOSFETs.

Apart from the explained differences, the switching behaviour of MOSFETs is very similar to that of IGBTs due to the equivalent gate structure.

As described in chapter 1.2.1, the forward on-state and forward off-state capability, the reverse behaviour and the limits of the transient currents and voltages during switching are influenced by the *internal structures of the bipolar transistor* and the *lateral resistances*.

The switching behaviour (switching velocity, switching losses) of MOSFET and IGBTpower modules is determined by their structural, *internal capacitances (charges*) and the *internal and outer resistances*.
Contrary to the ideal of a powerless voltage control via the MOSFET or IGBTgate, a frequency-dependent *control power* is required resulting from the necessary *recharge currents* of the internal capacitances, see chapter 3.5.
Moreover, the commutation processes are affected by the *parasitic connection inductances* existing in the power layout and generated by connection of transistor chips in power modules; they induce transient overvoltages and may cause oscillations due to the circuit and transistor capacitances (see chapter 3.4).

In the following, the switching behaviour of MOSFETs and IGBTs is to be analysed in relation to the internal capacitances and resistances of the transistor.

When the MOSFET (IGBT) is turned off, C_{GD} (C_{GC}) is low and is approximately equal to C_{DS} (C_{CE}).
During on-state C_{GD} (C_{GC}) will increase rapidly due to inversion in the enhancement layer below the gate zones, as soon as the gate-source (emitter) voltage has exceeded the drain-source (collector-emitter) voltage.
Additionally, C_{GD} (G_{GC}) will increase dynamically during the switching procedure due to the Millereffect:

$C_{GDdyn} = C_{GD} (1- dv_{DS}/dv_{GS})$ (MOSFET)
$C_{GCdyn} = C_{GE} (1- dv_{CE}/dv_{GE})$ (IGBT)

In most datasheets the following voltage-dependent low-signal capacitances of turned off transistors are given (see chapters 2.2.2, 2.2.3).

Power MOSFET	**IGBT**	
$C_{iss} = C_{GS} + C_{GD}$	$C_{iss} = C_{GE} + C_{GC}$	Input capacitance
$C_{rss} = C_{GD}$	$C_{rss} = C_{GC}$	Reverse transfer capacitance
$C_{oss} = C_{GD} + C_{DS}$	$C_{oss} = C_{GC} + C_{CE}$	Output capacitance

For calculation of the switching behaviour, these datas may only be applied to a certain extent, since e.g. C_{iss} and C_{rss} will again increase enormously in a fully switched on transistor ($V_{DS} < V_{GS}$ bzw. $V_{CE} < V_{GE}$), a fact that is not considered in most datasheets (Figure 1.12 and Figure 1.13) [277].

Therefore, switching times in relation to gate current, drain-source voltage and drain current are determined with the aid of the MOSFET “gate charge characteristic” indicated in the datasheets, plotting the gate-source voltage over the gate charge Q_G on condition of “rated current” and 20 % or 80 % of the maximum drain-source voltage (Figure 1.12).
Load conditions and measurement circuit are equivalent to Figure 1.11. However, for simplification purposes, constant current is supposed to be fed to the gate.

Now, switching intervals may be determined very simply with the following relation (see chapter 3.5.1):

$i_G = dQ_G/dt$

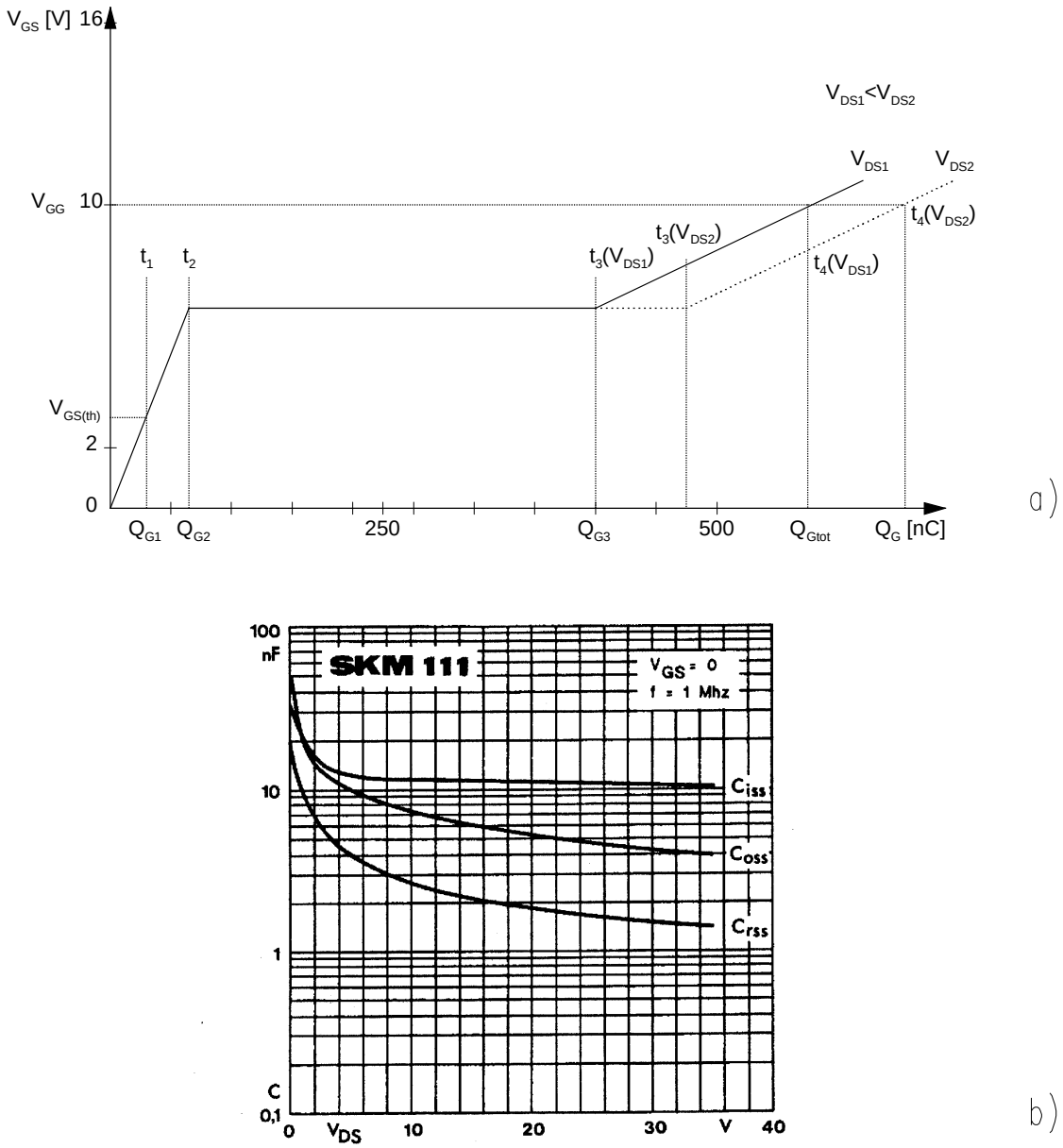


Figure 1.12 a) Gate-source voltage characteristic (V_{GS}) of a power MOSFET dependent on the gate charge Q_G (gate charge characteristic)
b) Low-signal capacitances of a power MOSFET

Turn-on: switching interval 0...t_1 (blocked transistor)

Gate current will be triggered by applying a control voltage.
Up to the charge quantity Q_{G1} the current i_G solely charges the gate capacitance C_{GS}. The gate voltage V_{GS} rises. As V_{GS} is still below the threshold voltage $V_{GS(th)}$, no drain current will flow during this period.

Turn-on: switching interval t_1...t_2 (rise of drain current)

As soon as V_{GS} has reached $V_{GS(th)}$-level at t_1, the transistor is turned on, first passing the *active region* (see chapter 1.2.2.1).
Drain current rises to I_L-level (ideal free-wheeling diode) or even exceeds I_L - as indicated in Figure 1.11a for a real free-wheeling diode. Similarly, V_{GS}, which is connected to the drain

current in the active region by the transconductance g_{fs} with $I_D = g_{fs} * V_{GS}$, will increase up to the value $V_{GS1} = I_D/g_{fs}$ (time t_2).
Since the free-wheeling diode can block the current only at t_2, V_{DS} will not drop considerably up to t_2.
At $t = t_2$ charge Q_{G2} has flown into the gate.

Turn-on: switching interval t_2...t_3 (transistor during turn-on)

When the free-wheeling diode is turned off, V_{DS} will drop almost to on-state value $V_{DS(on)}$ by time t_3. Between t_2 and t_3 drain current and gate-source voltage are still coupled by transconductance; therefore, V_{GS} remains constant. While V_{DS} is decreasing, the Miller capacitance C_{GD} is recharged by the gate current i_G with the charge quantity (Q_{G3}-Q_{G2}). By $t = t_3$ charge Q_{G3} has flownflown? into the gate.

Turn-on: switching interval t_3...t_4 (ohmic characteristic area)

At t_3 the transistor is turned on, its curve has passed the pinch-off area to enter the ohmic area. V_{GS} and I_D are no longer coupled by g_{fs}.
The charge conducted to the gate (Q_{Gtot}-Q_{G3}) at this point affects a further increase of V_{GS} up to the gate control voltage V_{GG}. Since the drain-source on-resistance $R_{DS(on)}$ depends on I_D and V_{GS}, the on-state voltage $V_{DS(on)} = I_D * R_{DS(on)}$ may be adjusted to the physical minimum by the total charge quantity Q_{gtot} conducted to the gate.
The higher the drain voltage V_{DD} (or commutation voltage), the bigger the charge Q_{gtot} required to reach a certain gate-source voltage, see Figure 1.12.

Turn-off

During turn-off the described processes are running in reverse direction; the charge Q_{Gtot} has to be conducted out of the gate by the control current.
For approximations to determine the gate charge quantity required for turn-off, the gate charge characteristic in Figure 1.12 may be used.

The further the specific transistor application deviates from the „hard switch“-application described, the more the step-form of the gate-source voltage blurs. The intervals „decoupled“ by the free-wheeling diode during hard switching will then more or less merge into one another, which requires a more complex explanation of the switching behaviour. [278].

The above-mentioned description may be applied to IGBTpower modules by analogy. The switching behaviour can be determined correspondingly by the gate charge characteristic also indicated in the datasheets.
Since an IGBTgate is mostly switched between a positive and a negative gate voltage, also a certain charge quantity is required to switch the gate capacitance between 0V and V_{GG}-. Therefore, the gate charge characteristic has to be extended as depicted in Figure 1.13. to calculate the total gate charges.

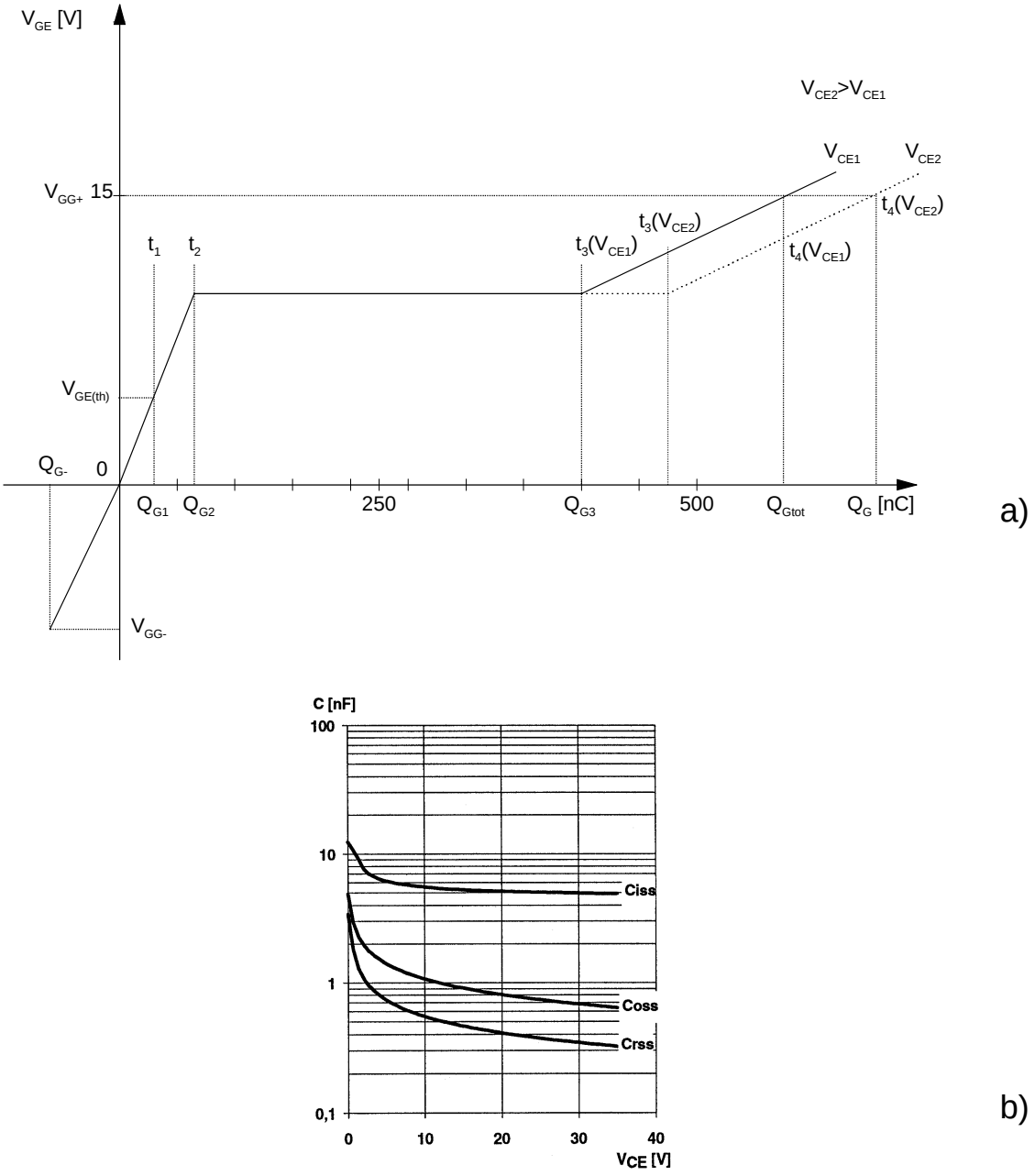


Figure 1.13 a) Extended IGBT gate charge characteristic for gate control between V_{GG+} and V_{GG-}
b) IGBT low-signal capacitances

1.2.4 New developments in MOSFET and IGBT technology

For the time being, the most important goals in research and development of MOSFET- and IGBT chips are:

a) Reduction of the on-state voltage
b) Reduction of switching power losses
c) Improved ruggedness (overcurrent-, overvoltage-behaviour, switching performance)
d) Increased off-state voltage for high-volt transistors
e) Consequent to a)...c): increased current density (shrinking)
f) Provided that e) is complied with, increase of current per chip or decrease of chip surface and costs
g) Optimized *low saturation* and *high speed*-IGBTs

h) Integration of monitoring, protection and driver functions or power electronic circuits (monolithic, chip-on-chip or silicon-on-insulator)

Especially during the past years a rapid development progress is to be noted concerning mainly the optimization of the horizontal and vertical cell design, the refinement of the cell structure and the successful handling of ultra-thin silicon wafers.
With mastery of the thin-wafer technology (wafer thickness 100µm), for example, the production of extremely low-loss 600V-IGBTs in NPT-technology had been possible [164].

For the time being, the principal improvement potential for MOSFETs and IGBTs lies in optimizing the cell design.
Firstly, there are new superfine structures, such as the S-FET product range by SIEMENS, thanks to the latest self-adjusting processes realizing an on-state resistance that is a fifth of that of conventional MOSFETs and a clearly improved switching and avalanche stability [216]. These structures, which are applied in similar forms also in modern high-density IGBTs, contain double-implantation gates with spacers in the margin region (Figure 1.14).

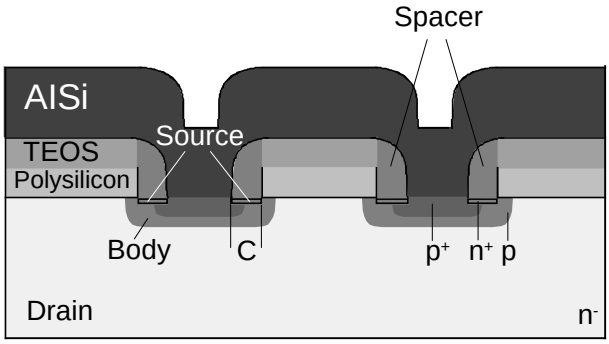


Figure 1.14 Double-implantation gate structure (Siemens S-FET) [298]

A lately developed gate structure for MOSFETs and IGBTs which will replace the conventional gate structure is the *trench-gate*, which allows for a vertical passage of the channel in the p-well (Figure 1.15). Since this structure provides for more active silicon surface, control of the channel cross-section becomes easier and a smaller channel resistance may be realized. The on-state losses can be reduced by about 30 %.
Furthermore, the cell surface can again be reduced, allowing higher current density, reduced on-state losses, improved latch-up stability, reduced switching losses and a higher breakdown voltage compared to planar MOSFETs and IGBTs.
The disadvantages, however, are a decreased short-circuit stability and an approximately three times higher gate capacitance compared to that of planar elements.

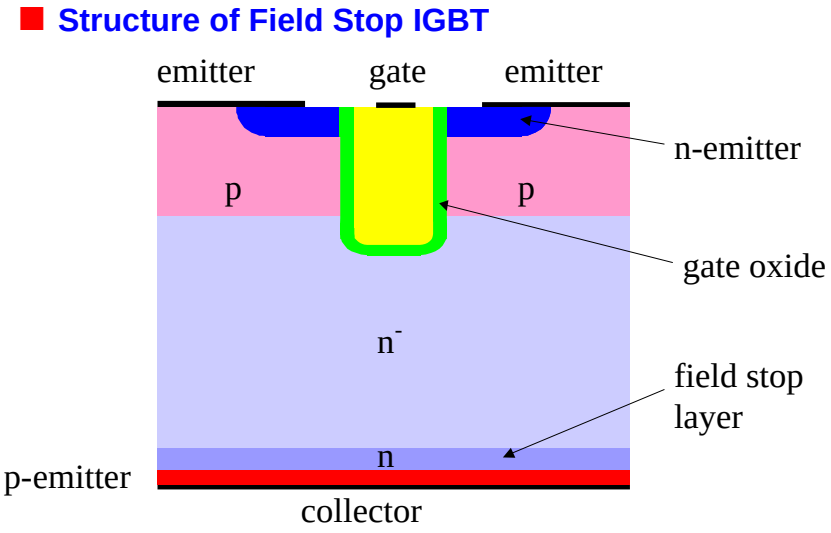


Figure 1.15 IGBT-cell with trench-gate and field stop layer

Also the so-called IEGTs (**I**njection **E**nhaced **G**ated **T**ransistors) for extremely high voltage applications (4.5...6.5 kV) have been designed in trench technology; due to the cathode emitter structure, the leak-off process of the holes is impeded, causing a charge carrier density similar to that of thyristors during on-state [194].

A remarkable progress within the high-volt power MOSFET has been made with the CoolMOS introduced by SIEMENS in 1998 [216]. As shown in Figure 1.16, the MOSFET-cell structure of the CoolMOS has been equipped with p-conducting areas in the drift zone which are connected to the p-wells.

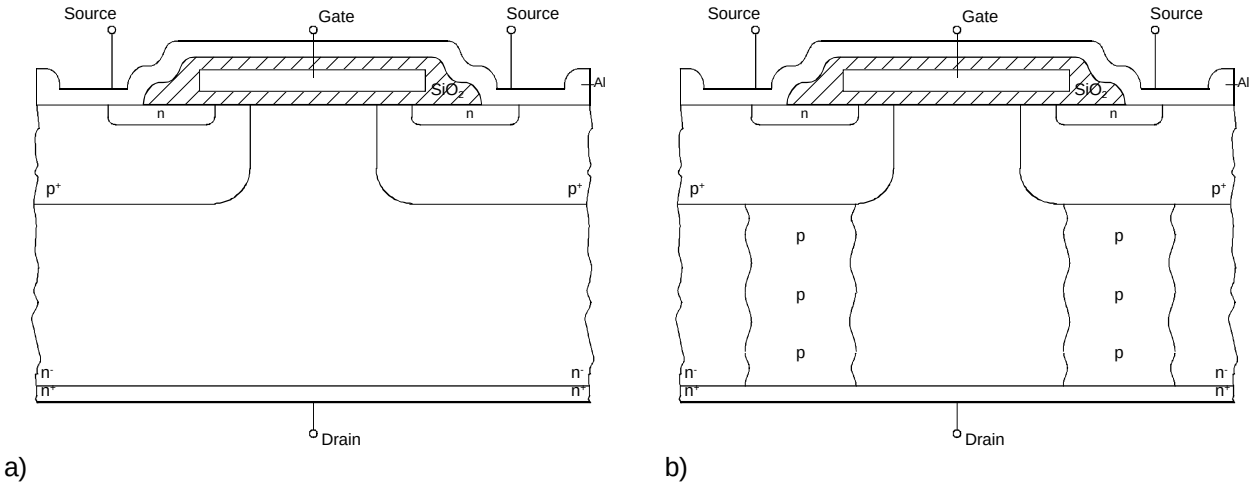


Figure 1.16 MOS- cell structures
a) Conventional structure
b) CoolMOS-structure (principle)

Since, during forward off-state, the electrical field is not only handled in vertical, but also in horizontal direction, the n^--drift area may be drastically reduced in size compared to conventional MOSFETs, by increasing its conductivity at the same time.
The turn-on resistance $R_{DS(on)}$ will then not increase in the exponential way described under chapter 1.2.1 anymore (exponent 2.4...2.6), but only linearly to the breakdown voltage $V_{(BR)DS}$.

By this, the forward on-state losses of a 600V-CoolMOS, for example, will be reduced by the factor 5 in contrast to a conventional MOSFET with the same chip surface. Only 1/3 of the previous chip surface is required to manage the same current. Switching losses will be halved and on-state losses will be reduced to about 35 %; due to the reduced chip surface, also gate capacitance and gate charge will decrease to about a third of the previous value [216].
However, the bad dynamic behaviour of the inverse diodes inside the CoolMOS-structure is disadvantageous. This restricts the application in hard switching topologies with inductive commutation.
Further progress will be achieved with the use of other semiconductor materials, such as silicon carbide (SiC).
Compared to Si, SiC shows an almost 10 times higher breakdown field intensity.
In spite of restricted mobility of the electrons, on-state resistances reduced by the factor 1/300 are realizeable in unipolar components, which guarantees for a high-voltage application range far beyond 1000V. As for bipolar SiC-components, the smaller drift area results in a scaled down storage charge. On the one hand, the energy gap, which is three times as big as that of Si, allows operating temperatures up to 500°C; on the other hand the threshold voltage of bipolar components is increased to 2.5V.
Other unfavourable effects lie in the considerably higher junction capacitances compared to Si-components and in today's still tremendous technological problems: diffusion of impurity centers is almost impossible, non-defective big surfaces are currently not realizeable and today's fundamental technologies for the margin design are not applicable to SiC. [282], [124], [130].

The integration of monitoring, protection and driver functions or power electronic circuits (monolithic, chip-on-chip or silicon-on-insulator) to the chip is more and more gaining importance in low-voltage (e.g. car electronics) or low-current (e.g. consumer products) batch applications.
For example, driver-, protection-, system- and diagnostic functions have been integrated on one chip in the „intelligent" SMARTPOWER-transistors, leading to a reduction of power losses and to an improvement of the system reliability apart from the advantages of system miniaturization [277], [213], [232].

The simplest method is to generate e.g. protection- and sensor units to manage currents, voltages or temperatures on control supply potential by diffusion to the MOSFET- or IGBT-chip surface.
Popular designs to be mentioned are the *SENSFET* and the *Sense-IGBT*, where source- or emitter current, respectively, are separated into a main circuit conducting the main current share and a parallelled measuring circuit. By inverse feedback of the measuring signal to the control circuit, the measuring current is reduced by increase of the sense-resistance [194]. Sense-IGBTs are integrated in many IPMs.
The *TEMPFET* is equipped with an integrated temperature sensor, which is used as overcurrent indicator at the same time and which will short-circuit the gate-source-connection, in case a certain temperature limit has been exceeded.

*PROFET*s and *HITFET*s, for example, contain a complete driver circuit with overcurrent-/short-circuit-protection, overvoltage- and overtemperature-protection, gate-protection, load indicator, polarity protection, over- and undervoltage turn-off and a charge pump for generation of the gate voltage, e.g. [4], [277].
The *PROFET* is being produced as single- and multi-channel high-side switch up to a break-over voltage of 60V.
In contrast to the high-side switch, there is not sufficient supply voltage generated for the protection logic during on-state of a MOSFET for a low-side switch. Therefore, an integrated

temperature sensor in the *HITFET* will reduce the gate voltage at a high chip temperature that the drain voltage is able to increase to the minimum supply voltage-value of 3V and the protection circuit may react.
With reference to [232], *monolithic integration* of whole inverters with power semiconductors, high-voltage ICs for driver/ protection and micro-electronic system control circuits is limited to 1A/ 600V (soon up to approx. 2A) and 5A/75V for the time being, the disadvantages compared to hybrid system integration of chips (currently up to 30A/ 1200V and up to 150A towards the year 2002) being the limitation of the blocking voltage to 600 V, restricted ruggedness reffering to short-circuit- and pulse-currents and tripled losses in the used lateral transistors in contrast to vertical transistors.

1.3 Free-wheeling- and snubber-diodes

1.3.1 Demands to free-wheeling and snubber-diodes

Modern fast switching devices require fast diodes as free-wheeling diodes. With every turn-on of the switch, the free-wheeling diode is commutated from conductive to blocking state. At this process, it has to show soft-recovery behaviour. For a long time, the importance of fast diodes had been underestimated. The performance of the switch had been impaired by the free-wheeling diodes. During the past few years, however, free-wheeling diodes had regained importance, and significant progress could be made by improving the reverse-recovery behaviour.

1.3.1.1 Reverse voltage and forward voltage drop

The *reverse voltage* V_R indicates that, at a specified voltage, the leakage current must not exceed the limit current I_R.
The specifications in the databooks are indicated for an operating temperature of 25°C. In the case of lower temperatures, the blocking capability will decrease, e.g. by approximately 1.5 V/K for a 1200V-diode. For components which are operated at temperatures below the ambient temperature, this has to be considered in the circuit layout.

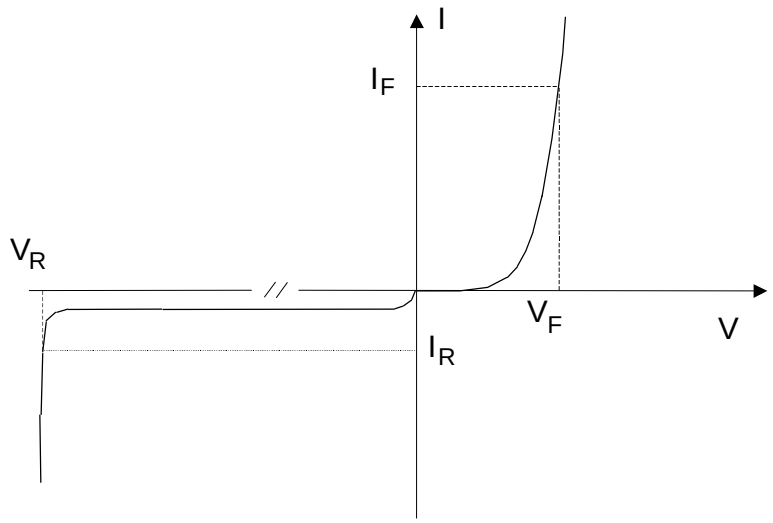


Figure 1.17 Definition of reverse and forward voltage of a diode

At temperatures above the ambient temperature the reverse voltage will increase accordingly, however affecting an simultaneous increase of the leakage current. Therefore, a leakage current

value is specified also for high temperatures (125°C or 150°C). In case of gold-diffused devices the leakage current can rise very steeply, which might cause thermal instability in circuits, where the whole system is operated at high temperatures due to the losses of the switching devices.

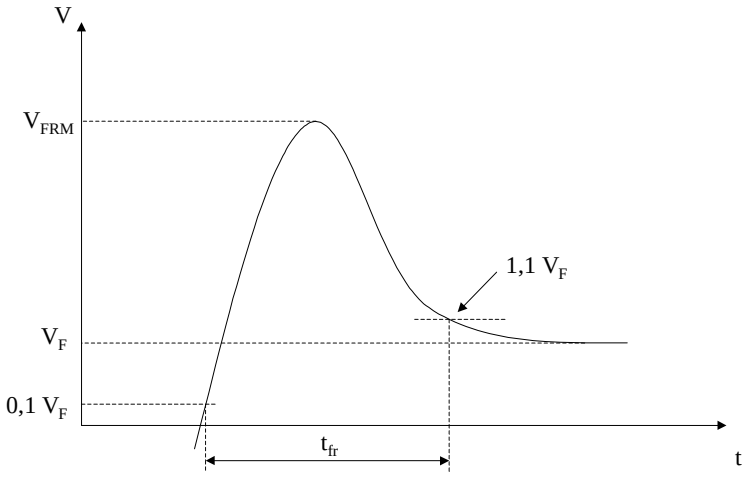


Figure 1.18 Turn-on behaviour of power diodes

The *continuous forward voltage* V_F indicates that, at a specified current, the forward voltage drop over the diode must not exceed the specified limit value. Typically, these limit values are specified at ambient temperature. A decisive factor in the power loss balance, however, is the forward voltage at higher temperatures. All datasheets of free-wheeling diodes should contain a note of this temperature dependency.

1.3.1.2 Turn-on behaviour

When the diode passes over to conductive state, the voltage will at first increase to the repetitive peak forward voltage V_{FRM}, before it drops to forward voltage level again. Figure 1.18 shows the currently valid definition of V_{FRM} and the turn-on time t_{fr}.
This definition, however, does not give much information on the behaviour of free-wheeling and snubber-diodes for IGBTs, because

- the rise of the on-state current di/dt is so high that e.g. V_{FRM} may increase to 200V or even 300V for an unsuitable 1700V-diode, which is more than 100 times V_F,
- the diode is normally turned on f run the blocking state, generating a considerably higher V_{FRM} than if it is turned on from its neutral state.

A low V_{FRM}-value is one of the most important requirements to snubber-diodes, since the snubber-circuit becomes effective only after turn-on of the diode.
The repetitive peak forward voltage is also of importance for free-wheeling diodes, which are designed for a reverse voltage of > 1200V. When the IGBT is turned off, a peak voltage is generated over the parasitic inductances, which is still superimposed by V_{FRM} of the free-wheeling diode. The sum of both components may lead to critical voltage peaks.
However, this measurement is not trivial, since the inductive component and V_{FRM} cannot be told apart in the application conform chopper circuit. Measurements may only be made with the open construction directly at the bonding wires of the diode.

On the other hand, turn-on behaviour of a diode is not important for the power loss balance, since turn-on losses only amount to a small percentage of the losses during turn-off and forward on-state and may therefore be neglected.

1.3.1.3 Reverse recovery behaviour

When passing over from the conductive to the blocking state, the internal diode storage charge has to be discharged. This results in a current flowing in reverse direction in the diode. The waveform of this current is characterized as the reverse-recovery behaviour.
Figure 1.19 shows the simplest circuit for the characterisation.

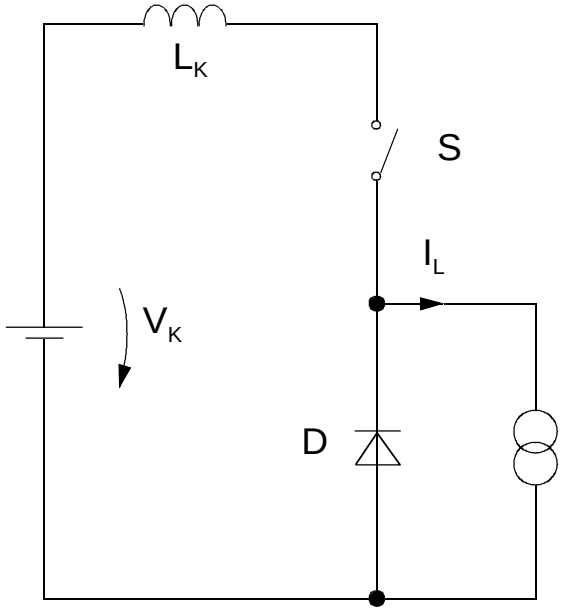


Figure 1.19 Reverse-recovery test circuit

S depicts an ideal switch, I_L is the current source, V_K a voltage source and L_K stands for the commutation circuit inductance.

After closing switch S, a soft-recovery diode will show a current and voltage characteristic as shown in Figure 1.20. Figure 1.20 is an example for a soft-recovery behaviour of a diode.

Figure 1.21 shows two examples for diode current characteristics with snappy switching behaviour. Firstly, the definitions are explained by referring to Figure 1.20.

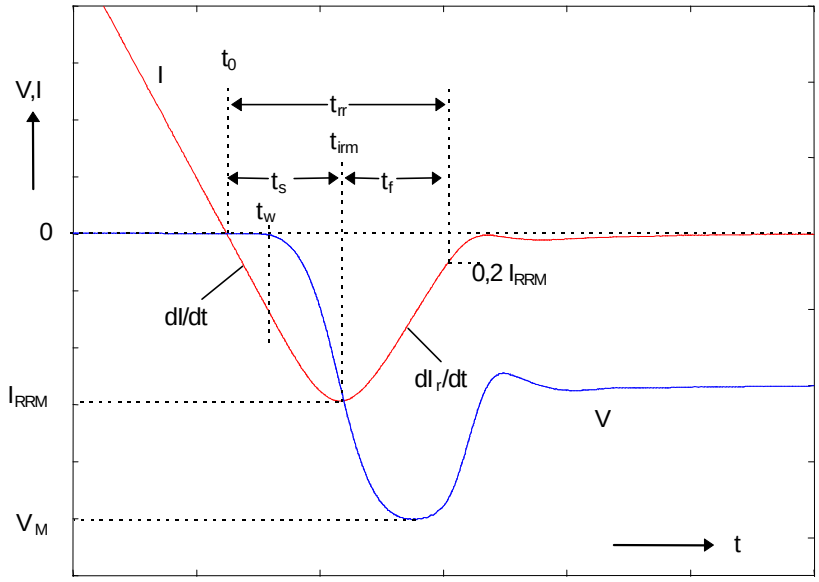


Figure 1.20 Current and voltage characteristic of the reverse recovery process of a soft-recovery diode in a circuit as shown in Figure 1.19 and definition of the characteristics of the recovery behaviour

The commutation velocity dI/dt is determined by voltage and inductance:

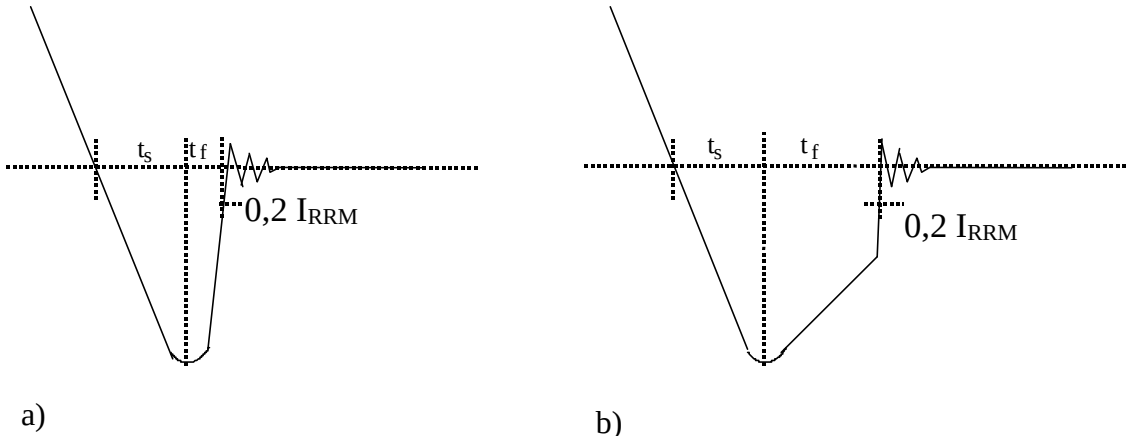
$$-\frac{dI}{dt} = \frac{V_K}{L_K} \tag{1.1}$$

At t_0 current is at zero passage. At t_w the diode starts to block. At this instant, the pn-junction in the diode gets free of charge carriers. At t_{irm} the reverse current is at its maximum I_{RRM}.
After t_{irm} the current will fall to leakage current level, the current characteristic depends solely on the diode. If the current drops very steeply, this is called snappy recovery behaviour. If the current drops very softly, this is called soft recovery behaviour.

The reverse recovery time t_{rr} is defined as the time between t_0 and the time, where the current has dropped to 20 % of I_{RRM}. The subdivision of t_{rr} into t_f and t_s shown in Figure 1.20 defines as quantitative value for the recovery behaviour:

$$\text{Soft factor} \quad s = \frac{t_f}{t_s} \tag{1.2}$$

This definition is insufficient, because, as a consequence, the current characteristic as in Figure 1.21a would be snappy. The characteristic in Figure 1.21b, however, would be classified as soft even though $t_f > t_s$ holds, there is a hard snapp-off.



a) b)

Figure 1.21 Current characteristic for two different possibilities of snappy reverse recovery behaviour

Better is the definition:

Soft-factor
$$S = \left| \frac{-\frac{dI}{dt}\Big|I = 0}{\left(\frac{dI_r}{dt}\right)_{max}} \right| \tag{1.3}$$

Measurements have to be taken at a current flow of less than 10 % and of 200 % of the specified current. By this also the charactertistic in Figure 1.21b will be defined as snappy.
Moreover, this considers that small currents are extremely critical for the reverse-recovery behaviour.
The occurring overvoltage is determined by dI_r/dt according to the inductance law

$$V_{ind} = -L_K \cdot \left(\frac{dI_r}{dt}\right)_{max} \tag{1.4}$$

Therefore, overvoltage occurring under certain measuring conditions or the peak voltage $V_M = V_K + V_{ind}$ may also be seen as characteristics for the recovery behaviour. V_K and dI/dt have to be figured in this context.
But also this definition is not sufficient, because it still neglects the following parameters:

1. Temperature. Mostly, high temperatures have a negative influence on the recovery behaviour. But for certain fast diodes, the recovery behaviour will get worse at ambient temperature or at lower temperatures.
2. Applied voltage. Higher voltages will lead to impaired reverse recovery
3. Rate of rise of commutation current dI/dt. The dependency on dI/dt is very different for diodes of various manufacturers. Some types of diodes react more softly with increase of dI/dt, other types behave more snappy.

All these different influences may not be summarized in one simple definition of quantity. Therefore, the circuit in Figure 1.19 and the definitions according to (1.2) or (1.3.) are only usefull to explain the effects of the single production parameters of diode behaviour. An overall estimation of reverse recovery behaviour can only be made under application-related conditions.
An application-related measuring circuit is shown in Figure 1.22.

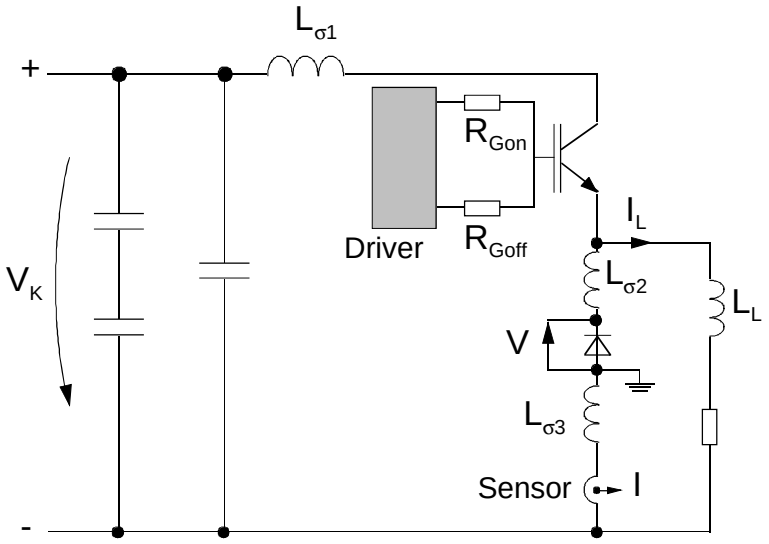


Figure 1.22 Application-related chopper circuit of a step-down converter (double-pulse operation) for reverse recovery measurements

The commutation velocity dI/dt is adjusted by the gate resistor R_{Gon} of the switching device. V_K is the DC-link voltage. A parasitic inductance $L_{\sigma 1}$ is generated in the connections between capacitors, IGBT and diode. Figure 1.23 shows the IGBT control signals and the current flow within IGBT and diode under double-pulse operation. By turn-off of the IGBT, the load current will be taken over by the free-wheeling diode. As soon as the IGBT is turned on next time, the diode will be commutated, characterizing its recovery behaviour at that moment. During turn-on, the IGBT also takes over the reverse current of the free-wheeling diode. This procedure is depicted for a soft-recovery diode in Figure 1.24 at a higher resolution of the time axis. Figure 1.24a shows an IGBT current and voltage characteristic and also the turn-on power losses. Figure 1.24b shows the FWD-current and voltage characteristic as well as power losses.

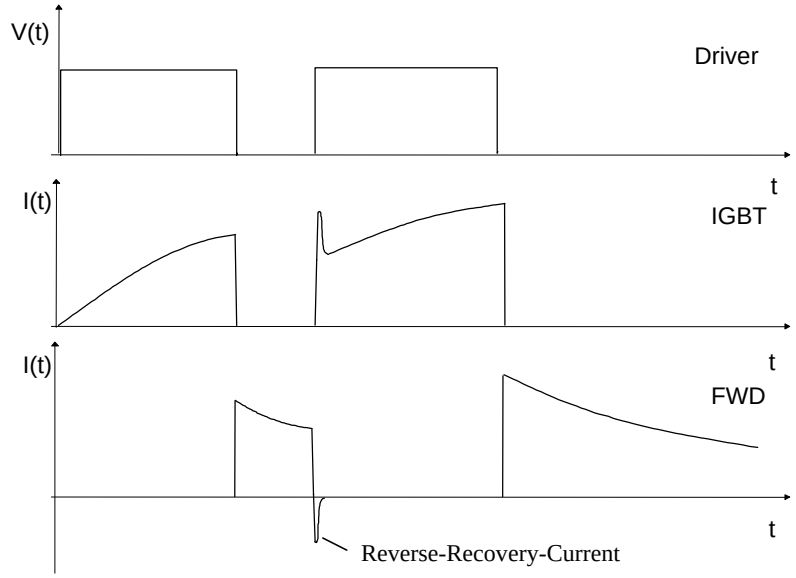


Figure 1.23 Driver control signal, IGBT- and FWD-current waveforms in a circuit according to Fig. 1.22 (double-pulse operation)

While the IGBT conducts the peak reverse current I_{RRM}, the IGBT-voltage is still on DC-link voltage level (1200V in Figure 1.24a). This is the moment of maximum turn-on losses in the IGBT.
The diode reverse recovery characteristic may be divided up into two phases:

1. The phase of increase up to the reverse peak current and the consequent reverse drop current with dI_r/dt. dI_r/dt is within the range of dI/dt as far as a soft-recovery diode is concerned. The peak reverse recovery current I_{RRM} exerts most stress on the switching device.

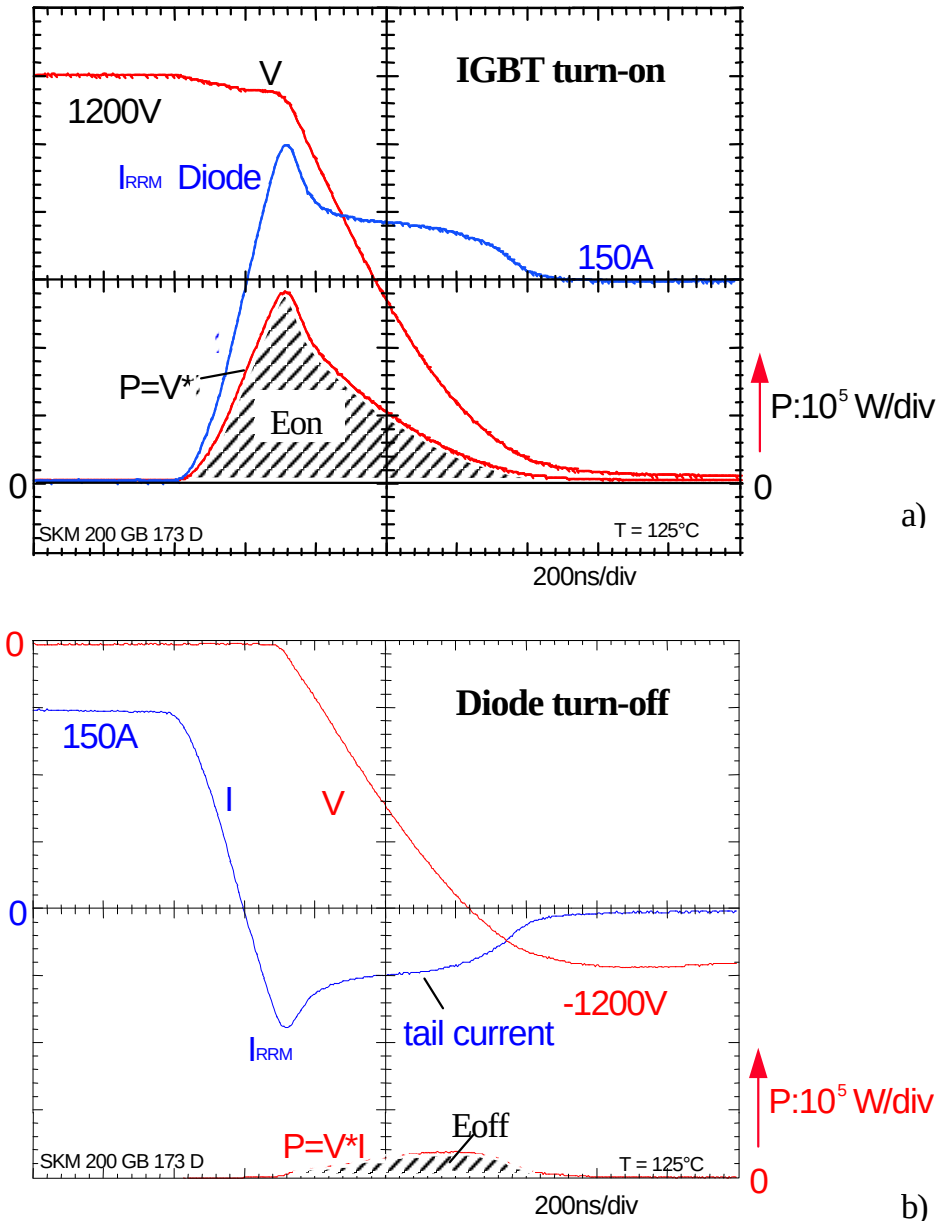


Figure 1.24 Current, voltage and power losses during IGBT turn-on (a) and diode turn-off (b) for a measurement in a test circuit according to Figure 1.22

2. The tail phase, where the reverse current slowly declines to zero. There is no point in defining a t_{rr}. The main power losses in the diode are due to the tail phase, where voltage has already been applied to the diode. A snappy diode without tail current would cause less

switching losses, but would be unsuitable for the application. In the IGBT, the switching losses during the tail phase are not that extreme, because the applied voltage has already decreased at that time.

Compared to IGBT switching losses, the losses the diode are low in the application (diode switching losses in Fig. 1.24b are drawn to the same scale as the IGBT switching losses in Fig. 1.24b). In order to keep power losses of both, IGBT and diode, as low as possible, it is important to care for a small peak reverse current and to have the main part of the storage charge discharged during the tail phase. A limit to this is set by the maximum switching losses that can be dissipated in the diode.
The peak reverse recovery current I_{RRM} is the most important parameter for the diode taking influence on the total losses. Therefor it should be minimized.
In a typical application, where the chopper is in a semiconductor module, the parasitic inductance $L_{\sigma ges}$ is in the range of 40nH, reducing the generated overvoltage. Due to lack of ideal switches, the voltage applied to the IGBT will drop to a certain degree during the recovery phase. The voltage taken becomes

$$-V(t) = -V_K - L_{\sigma ges} \cdot \frac{dI_R}{dt} + V_{CE}(t) \qquad (1.5)$$

with $V_{CE}(t)$ being the voltage still applied to the IGBT at the respective time. It is typical of soft-recovery diodes that, for moderate rates of rise up to 1500A/µs and minimized parasitic inductances, V(t) is smaller than V_K at any time and that there will be no voltage peaks.

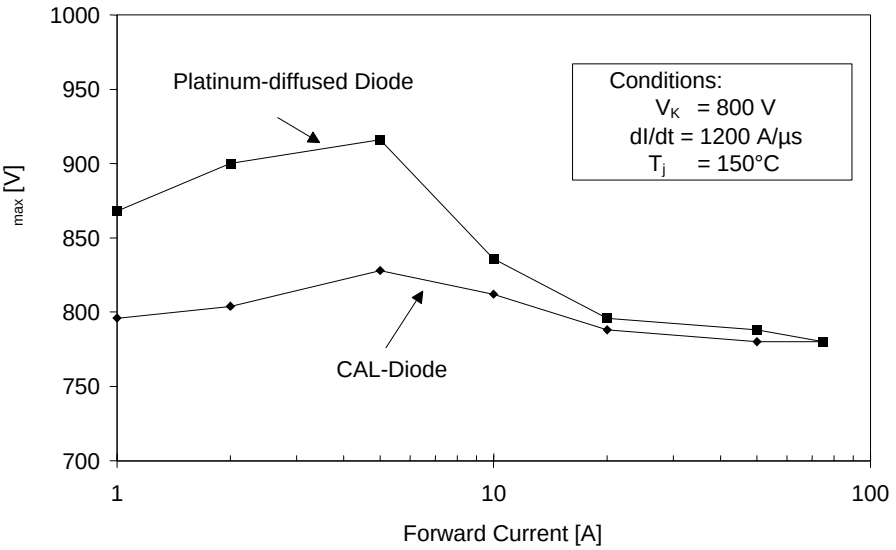


Figure 1.25 Peak voltage during commutation in dependence of forward on-state current as a parameter for the switching behaviour of diodes

Figure 1.25 gives an example for characterization of the recovery behaviour by this method. In these conditions, the overvoltage occurring in a CAL-diode has been compared to that occurring in a diode, the charge carrier life of which had been adjusted by platinum-diffusion, showing soft-recovery behaviour by reduced p-emitter efficiency. A platinum-diffused diode behaves as soft as a CAL-diode at rated current (75A). Smaller currents, however, will cause overvoltages up to a maximum of more than 100 V at 10 % of rated current due to snappy switching behaviour. Even smaller currents are switched more slowly by the applied IGBT, affecting a

decrease of overvoltage. In contrast to that, there will be no substantial overvoltage on any of those conditions with CAL-diodes.
All further explanations in this manual are based on the following definition:
A diode shows soft-recovery behaviour, if, in all conditions relevant to the application in an application-related circuit, no overvoltage occurs, caused by reverse current snap-off due to the diode.
Relevant conditions being the total current range, all commutation velocities useful for the application and the temperature range of -50°C up to +150°C. This definition is valid as long as dI/dt is not too high (> 6 kA/µs) or high parasitic inductances (> 50 nH) are applied, which might lead to circuit-dependent voltage peaks also with soft-recovery diodes.

An equally important requirement for free-wheeling diodes with a voltage from 100V upwards (apart from soft switching behaviour) is **dynamic ruggedness**. Figure 1.24b shows that nearly the whole DC-link voltage is taken up by the diode, while it is still conducting a substantial tail current. If the IGBT is switched very steeply (small gate resistance R_G), reverse current and tail current will rise, at the same time causing a decrease of V_{CE} at the IGBT, which switches over to the diode with a respectively higher dV/dt. The density of the current-carrying charge carriers (holes) will then be above the original doping density, the consequence of which will be an inevitable avalanche breakdown in the semiconductor at applied voltages far below reverse voltage level (dynamic avalanche). To manage these operating conditions is characteristic of the dynamic ruggedness of a free-wheeling diode. The dynamic ruggedness may be defined as follows:
The dynamic ruggedness is the ability of a diode to manage high rates of rise of commutating di/dt and a high DC-link voltage at the same time.
If the diode shows no sufficient dynamic ruggedness, manufactures limit the dI/dt of the IGBT or admit only a maximum reverse recovery peak current of the diode thus accepting increased switching losses.

1.3.1.4 Demands on free-wheeling diodes used in the rectifier and inverter mode of voltage source converters

Free-wheeling diodes in IGBT- or MOSFET-converters have to cope with different requirements depending on whether they are used in rectifiers or inverters with the same power regarding the power losses occurring.
Typically, the average energy flow in inverter mode is directed from the DC-link to the AC-side, i.e. a consumer is connected to and supplied by the AC-side (e.g. three-phase motor).
On the other hand, the average energy flow in rectifier mode is directed from the AC-side to the DC-link. In this case the converter works as a pulse rectifier connected to an AC-mains or generator.
Although the power performance in both cases is the same, the power semiconductors are subject to different power losses basically due to the opposite phase shift between voltage and current on the AC-side, when in rectifier or inverter operation.
This can be explained using to the basic circuit in Figure 1.26.

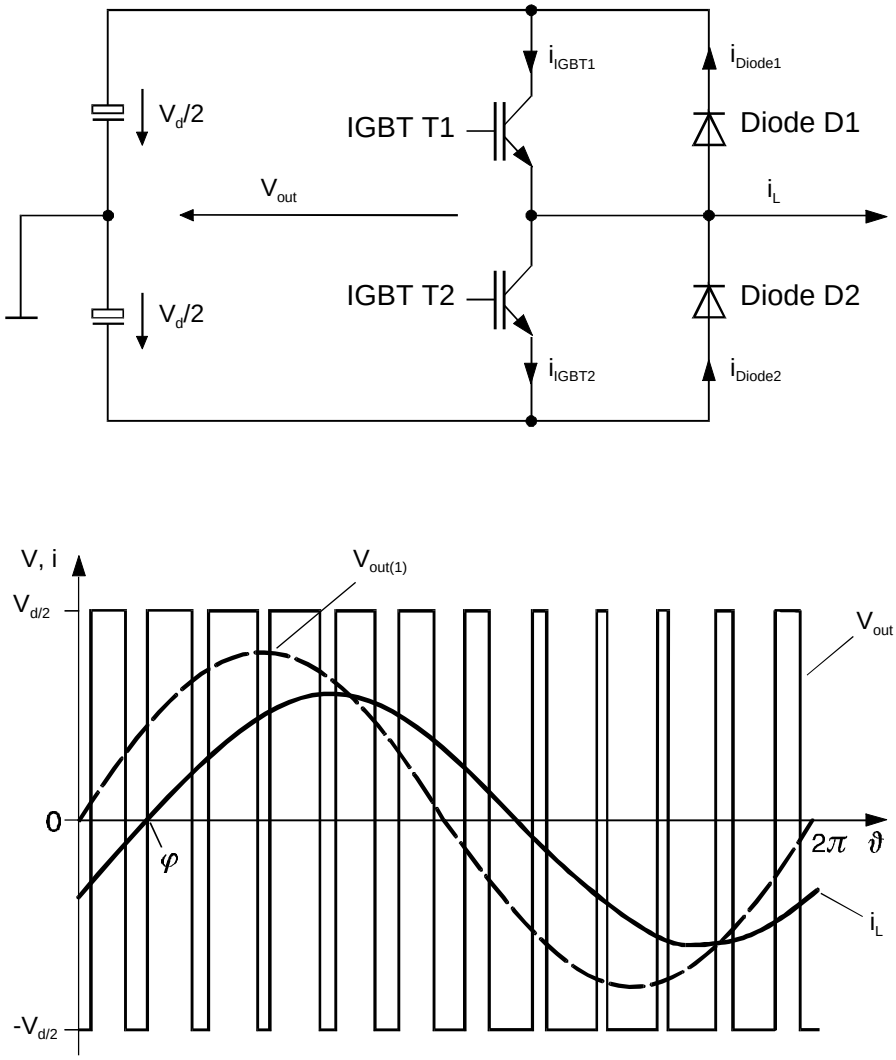


Figure 1.26 Basic circuit of a converter phase with IGBTs and free-wheeling diodes

It shows:

- if v_{out} = positive and $i_L > 0$: current flow over IGBT 1,
- if v_{out} = negative and $i_L > 0$: current flow over diode 2,

- if v_{out} = positive and $i_L < 0$: current flow over diode 1,
- if v_{out} = negative and $i_L < 0$: current flow over IGBT 2.

Consequently, the IGBT- and FWD- on-state power losses occurring at a given RMS-current value are dependent on the cos phi between voltage and current fundamental frequency as well as on the modulation factor m of the converter (determines duty cycles).

In the case of inverter-operation $0 \leq m*\cos\text{ phi} \leq 1$. Power losses in semiconductors reach their limits, if $m*\cos\text{ phi} = 1$. In this case maximum on-state losses and, therefore, total losses in the IGBTs have been reached, whereas losses in the free-wheeling diodes are at their minimum.

In the case of rectifier operation $0 \geq m*\cos\text{ phi} \geq -1$. Power losses in semiconductors reach their limits, if $m*\cos\text{ phi} = -1$. In this case, minimum on-state losses and, therefore, total losses in the IGBTs have been reached, whereas losses in the free-wheeling diodes are at their maximum. Applied to the characteristics in Figure 1.26, this situation is given when the fundamental

frequency of the pulse rectifier converts pure active power from the line and the neutral point of the line is connected to the centre point of the DC-link voltage.

This is illustrated with the graphs in Figure 1.27 with an example.

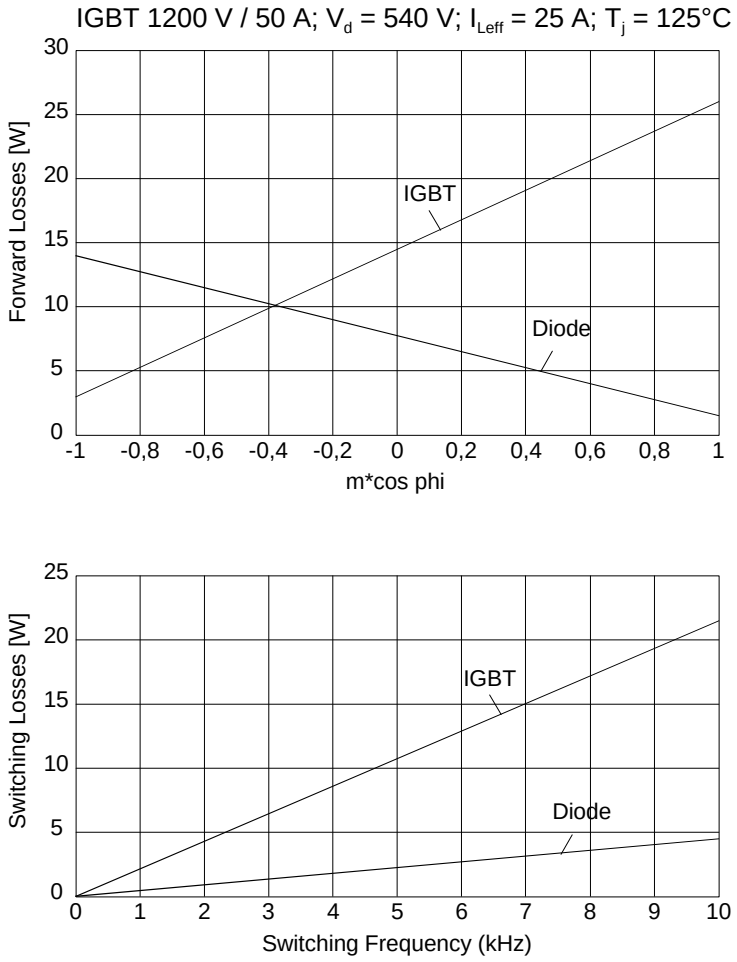


Figure 1.27 Switching and forward on-state losses of IGBT and free-wheeling diode in a VSI

At given DC-link voltage and RMS-AC-current values the switching losses of the components are merely dependent (linear) on the switching frequency (Figure 1.27).

A large number of the available IGBT and MOSFET modules with integrated free-wheeling diodes are dimensioned for being applied in inverters regarding the power losses that may be dissipated at rated current (e.g. cos phi = 0.6...1). Due to their reduced on-state and total losses, diodes have been designed for a considerably lower dissipation of power losses compared to IGBTs (ratio IGBT : diode ≈ 2..3:1).
Therefore, the use of power modules with higher rated current is recommended when dimensioning pulse rectifiers with the same converter power as a corresponding pulse inverter.

Example:
Driving system:

* Power supply (400 V/50 Hz) – pulse rectifier (f_s = 10..12 kHz) – DC-link – pulse inverter (f_s = 10..12 kHz) – three-phase motor (400 V/50 Hz/22 kW)

* Pulse rectifier with standard IGBT-modules (phase leg) ≥ 1200 V/100 A (T_c = 80°C)
* Pulse inverter with standard IGBT-modules (phase leg) ≥ 1200 V/75 A (T_c = 80°C)

This difference is not required for power modules with higher rated diodes.

1.3.2 Structure of fast power diodes

We have to distinguish between two basic types: Schottky-diodes and pin-diodes.
In Schottky-diodes, the metal-semiconductor junction serves as blocking junction. There is no diffusion voltage at the pn-junction as in pin-diodes; this guarantees a lower on-state voltage as with any pin-diode, provided the n^--zone is very thin. When passing over from conductive to blocking state, ideally only the space charge zone has to be charged. Due to this, the component is suitable for very high frequencies (> 100 kHz). This advantage is, however, restricted to voltages < ~ 100 V. In this range, the Schottky-diode is the appropriate free-wheeling diode for a MOS-transistor. If, on the other hand, the component is dimensioned for higher voltages,
- the on-state voltage will rise considerably, since w_B increases and only one sort of charge carriers is available (unipolar) and
- the leakage current will rise considerably, which will cause thermal instability.

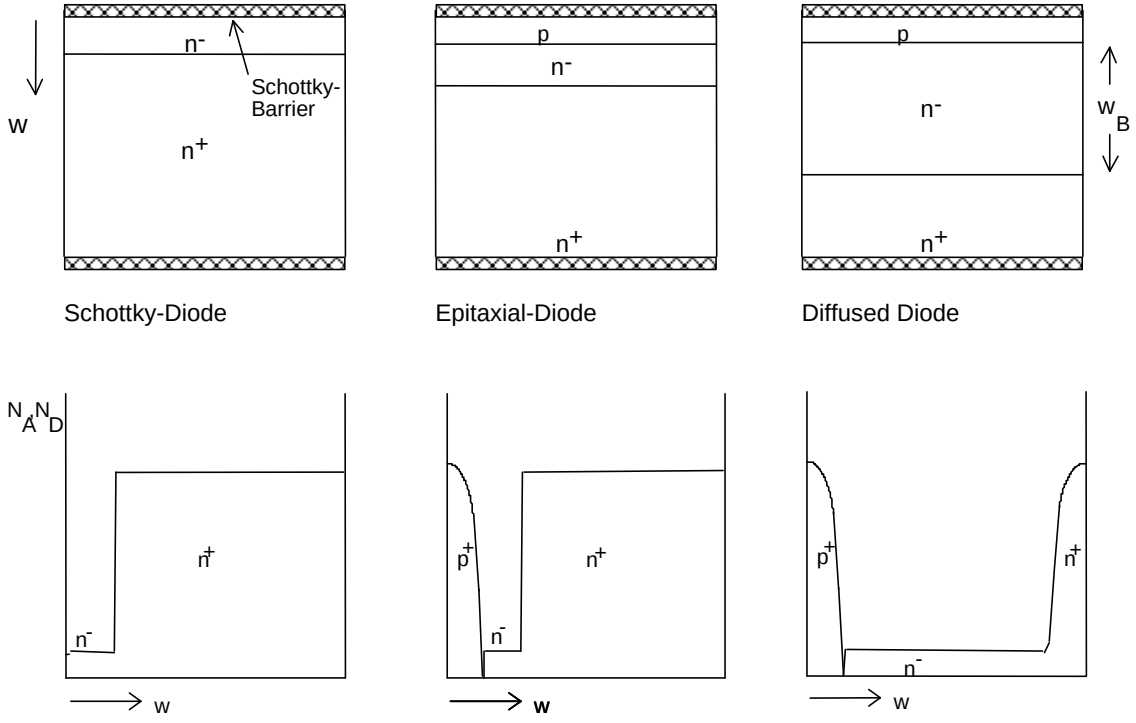


Figure 1.28 Schottky-, pin-epitaxial - and pin-diffused diode structures
Top: structure
Bottom: doping profile (scheme)

The advantages of pin-diodes become effective in the range of more than 100V. In diodes produced today, the middle zone is not „i“ (intrinsic), but of n-type with a very low doping level (n^-) compared to the marginal zones. In pin-epitaxial-diodes (Figure 1.28, mid) a n^--zone is separated from the highly-doped n^+-substrate (epitaxy). Then, the p-zone is diffused. By this technology, a very small base width w_B down to some µm may be produced, the silicon wafer being thick enough to manage high production yields. By diffusion of recombination centres

(mainly gold-diffusion) very fast diodes can nevertheless be produced with a low forward on-state voltage due to the small w_B. However, the on-state voltage will always be above the diffusion voltage of the pn-junction of 0.6 to 0.8 V. The main applications of epitaxial (epi-) diodes are within the range of 100 V and 600 V, some manufacturers are even producing epi-diodes for 1200 V.
From 600 V upwards the n^--zone will be enlarged to such an extent that a diffused pin-diode (right Figure) may be produced. The p- and n^+-zones are diffused into the n^--wafer. Similar, recombination centres are necessary to adjust the dynamical characteristic.
As the major applications of power modules are within the range above 100 V, pin-diodes will be explained in more detail in the following.

1.3.3 Characteristics of fast power diodes

As for free-wheeling diodes, a compromise has to be found for optimizing the contrasting requirements. Therefore, we have to come up against the physical limits of the material, which makes the design of excellent free-wheeling diodes very sophisticated.

1.3.3.1 Forward and blocking behaviour

In forward direction, there is the pn-junction and the resistance of the adjacent n^--zone. The voltage drop is composed of

$$V_f = V_{diff} + V_{ohm} \tag{1.6}$$

The pn-junction diffusion voltage V_{diff} is dependent on the doping of both pn-junction sides and is, typically, between 0.6...0.8V. For fast diodes with a blocking voltage of 600V and more, the ohmic part prevails. Charge carrier lifetime of free-wheeling diodes has to be kept very low so that the on-state voltage will depend exponentially on the base width w_B and the charge carrier lifetime τ [283]:

$$V_{Ohm} = \frac{3\pi kT}{8q} e^{\frac{w_B}{2L_A}} \tag{1.7}$$

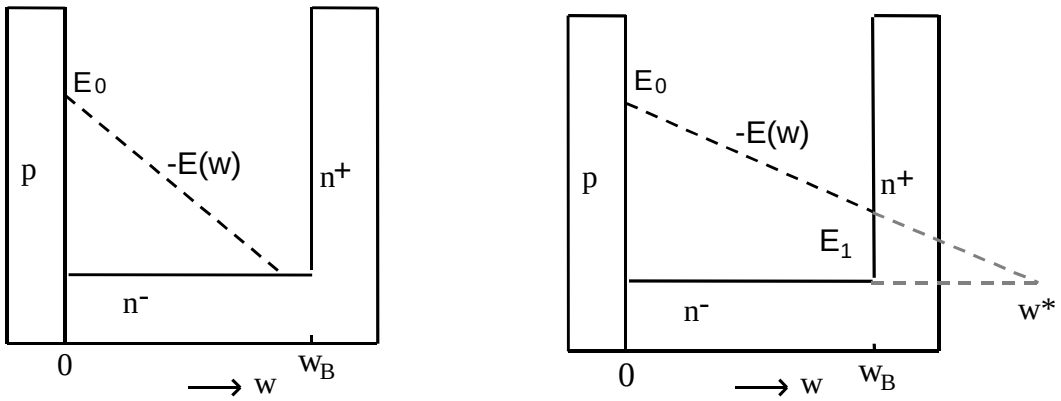
L_A is the ambipolar diffusion length

$L_A = \sqrt{D_A \tau}$, with the ambipolar diffusion constant $D_A = 2\frac{\mu_n \mu_p}{\mu_n + \mu_p}\frac{kT}{q}$.

k: Boltzmann-constant; $1.38066 \cdot 10^{-23}$ J/K
q: electronic charge; $1.60218 \cdot 10^{-19}$ C

μ_n and μ_p stands for the mobility of the electrons and holes on condition of a n^--zone flooded by free electrons and holes [284]. Due to this exponential correlation, the smallest possible w_B should be selected.

In spite of this, the base width w_B has a definite influence on the blocking voltage. Two different cases may occur (see Figure 1.29):
If w_B has been dimensioned in such a way that the space charge zone cannot protrude into the n^+-zone (triangular characteristic), this is called non-punch-through structure [285]. If w_B has been dimensioned in such a way that the space charge zone will protrude into the n^+-zone, the characteristic will be trapezoidal, which will be called punch-through-diode. However, a real punch-through, where the space charge zone would reach the area of another doping type, is not realized in this case. Nevertheless, the designation has generally been accepted.



non-punch-through (NPT) -Diode a)

punch-through (PT) -Diode b)

Figure 1.29 Dimensioning of a diode for triangular (a) and trapezoidal (b) characteristic

For an ideal **NPT-diode** w_B is dimensioned so that it is located at the end of the triangular characteristic. If the doping is optimal, the minimum width for w_B would then be

$$w_B = 2^{\frac{2}{3}} C^{\frac{1}{6}} V_R^{\frac{7}{6}} \tag{1.8}$$

with $C = 1.8*10^{-35}\ cm^6V^{-7}$

Minimum doping necessary for PT-diodes can be calculated similarly. As a extreme, the characteristic would be rectangular, $E_1 = E_0$ (see Figure 1.29). Consequently,

$$w_B(\mathrm{PT, extreme}) = C^{\frac{1}{6}}\ V_{BD}^{\frac{7}{6}} \tag{1.9}$$

Compared to w_B of the NPT dimensioning (1.8):

$$w_B(\mathrm{PT, extreme}) = 2^{-\frac{2}{3}} w_B(\mathrm{NPT}) \cong 0.63 w_B(\mathrm{NPT}) \tag{1.10}$$

This extreme case, however, may not be achieved, but with the existing technology it may be approximated by

$$w_B(\mathrm{PT}) \cong 0.66 \cdot w_B(\mathrm{NPT}) \tag{1.11}$$

The difference between PT-structure according to (1.11) and NPT-structure according to (1.8) adds up to about 0.8 V on-state voltage, considering the necessary low charge carrier lifetime. Therefore, PT-structure should be preferred.

1.3.3.2 Turn-on behaviour

When the diode is turned on, it has to overcome the resistance of the low-doped base. Therefore, the turn-on peak voltage will increase proportionally to w_B. The turn-on peak voltage becomes critical, especially if a significant base width w_B has to be chosen due to a high blocking voltage over 1200V. In this respect, PT-diodes will show optimized turn-on behaviour.
Free-wheeling diodes always contain recombination centres. For free-wheeling diodes dimensioned for applications of 1200V and more, recombination centres that cause increase of the base resistance have to be avoided. A like recombination centre would be one that had been generated by gold-diffusion. Recombination centres generated by platinum-diffusion, electron

beam radiation or light ions will only slightly increase the turn-on overvoltage in comparison to diodes without recombination centres.

1.3.3.3 Turn-off behaviour

The turn-off behaviour of fast diodes is determined by the way in which the charge declines to zero. Figure 1.30 shows the procedure for a snappy diode, Figure 1.31 for a soft-recovery diode.

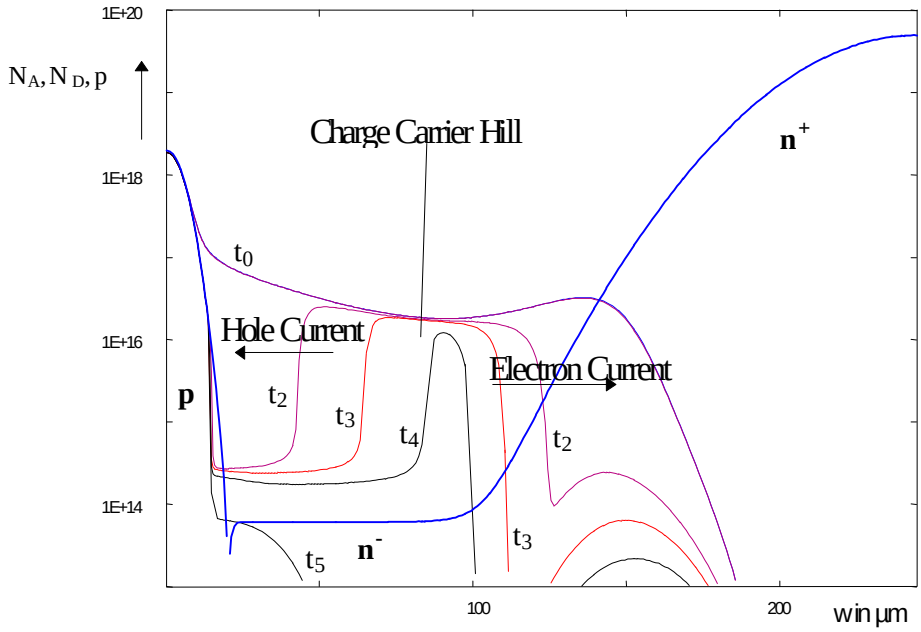


Figure 1.30 Diffusion profile and decline of charge carriers (density of holes) in a snappy diode (ADIOS-simulation)

During on-state, the n^--zone is flooded by > 10^{16} cm^{-3} electrons and holes, the concentration of electrons n and holes p presumably being the same. After commutation the charge carrier hill is within the n^--zone between t_2 and t_4, provided $n \approx p$. The decline of charge carriers towards the cathode is effected by the flow of electrons, that move towards the anode by the flow of holes, which flow as reverse current in the outer circuit. In case of the snappy diode in Figure 1.30 the charge carrier hill declines to zero shortly after t_4. Between t_4 and t_5 the diode will suddenly turn from its state with charge carrier hill to a state without charge carrier hill, the reverse current snaps off. The switching behaviour of the diode is snappy.

Figure 1.31 shows the same procedure for a soft-recovery diode. A charge carrier hill feeding the reverse current is kept during the whole procedure. At t_5 the diode has already taken on the applied voltage. The procedure described in Figure 1.31 will lead to a tail current as shown in Figure 1.24.

Whether soft-recovery behaviour is reached or not, depends on the successful reduction of charge carriers. This is difficult to achieve by microstructures on the surface, a technology where the semiconductor industry has made an enormous progress in the past. Therefore, it has taken a relatively long period of time until the reverse recovery behaviour could be controlled.

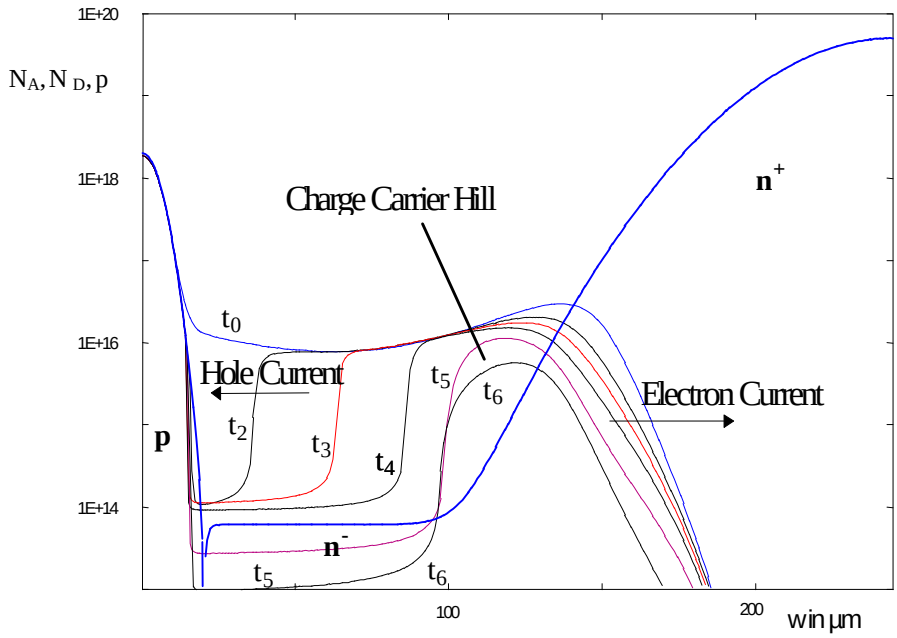


Figure 1.31 Diffusion profile and decline of charge carriers (density of holes) in a soft-recovery diode (ADIOS-simulation)

The following measures will effect a softer recovery behaviour:

1. The basis width w_B of the n^--zone is enlarged, NPT-dimensioning is applied (see equation (1.9)), an additional zone is generated in the diode, which is not reached by the field at rated voltage. But this will lead to extreme increase of the on-state voltage (see equation (1.7)) or the V_F/Q_{RR}-ratio. Nevertheless, this inconvenience is accepted even in lately developed solutions (as mentioned e.g. in [286]).
2. In order to slightly neutralize the w_B-increase, a two-phase n^--zone may be applied [287] showing a highly doped area near to the nn^+-junction. In Figure 1.30 and 1.31 a similar effect is realized by a flat gradient at the nn^+-junction. This measure on its own will not be sufficient in order to reach soft-recovery behaviour.
3. Inversion of the charge carrier distribution by a low-efficiency p-emitter (see chapter 1.3.4.1).
4. An axial charge carrier lifetime profile, providing for a low charge carrier life at the pn-junction, and a longer charge carrier life at the nn^+-junction (see chapter 1.3.4.2).

To guarantee for soft-recovery behaviour on any condition, usually several of those measures have to be taken at the same time. Progress in this respect has always to be assessed on consideration of the acceptance of a high on-state voltage drop or a higher Q_{RR}.

1.3.3.4 Dynamic ruggedness

While the space charge zone is increasing, a hole current, carrying I_R, is flowing through the empty area of the n^--zone. Therefore, the density p of the holes is:

$$p = \frac{I_R}{q v_d A} \tag{1.12}$$

In this equation, v_d stands for the drift velocity ($7.57 * 10^6$ cm/s) and A for the area of the diode.

The hole density (shown in Figure 1.30 and 1.31 from t_2 to t_4 each) must no longer be neglected with respect to the basic doping level [288]. P is added to the positively charged donators N_D, the effective doping N_{eff} at that moment is

$$N_{eff} = N_D + p \tag{1.13}$$

This will cause premature avalanche breakdown. Electrons and holes will be generated at the pn-junction by **dynamic avalanche**. The holes will move through the highly doped p-zone. On the other hand, the electrons will move through the n^--zone, causing an effective doping

$$N_{eff} = N_D + p - n_{av} \tag{1.14}$$

Here, n_{av} stands for the density of the electrons generated by dynamic avalanche, which move from the pn-junction through the space charge zone, partly compensating the hole density and thus counteracting the avalanche effect. In [289] dynamic avalanche is designated as a self-limiting effect: it is limited to a degree which is just sufficient to manage the field intensity resulting from the reduced effective doping. Consequently, the diode is not likely to be destroyed by dynamic avalanche.
Reduced forward current will cause reduced reverse current, and consequently reduced density of holes p (according to (1.12)). But, since the switching devices have a higher dV/dt at smaller currents, stress caused by dynamic avalanche may be higher, if small currents are applied.
For diodes dimensioned for higher blocking voltages, τ has to be increased due to the enlarged $w_{B.}$ This will cause higher reverse currents, leading to increased hole density and to dynamic avalanche according to (1.12). But dynamic ruggedness is especially important for the application in this case.

1.3.4 Modern diodes with optimized recovery behaviour

1.3.4.1 Emitter conception

In the conventional pin-diode the pn-junction is flooded by more charge carriers than the nn^+-junction (Figure 1.30). The idea of the emitter conception is to invert the charge carrier distribution: the nn^+-junction is to be flooded by more charge carriers than the pn-junction. This is achieved by reducing the injection quantity at the p-emitter.

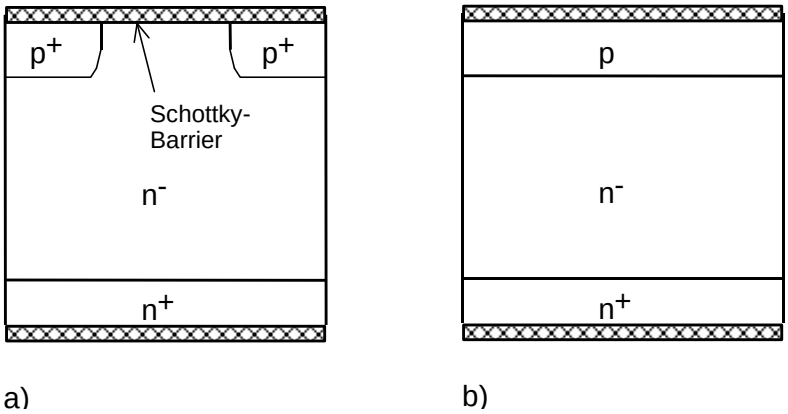


Figure 1.32 P-emitter for improvement of soft-recovery behaviour:
a) Emitter structures, e.g. the merged PiN/ Schottky diode
b) Reduced p-doping

Various emitter structures had been considered, which, in summary, would meet this effect by their functions. One example is the ”merged PiN/Schottky-diode”, consisting of a sequence of p^+-zones and Schottky-areas [290] (Figure 1.32a). There is a number of structures similar to that, comprising also structures with diffused p- and n-zones.
The advantages of Schottky or similar zones, however, are restricted to voltages below 600V. As for blocking voltages of 1000 V and more, the ohmic potential drop will prevail. Only the reduced injection area at the p-zone remains. The same effect as with emitter structures is achieved by a continuous low-doped p-zone (Figure 1.32b). On balance the result of the application of these structures is that they have not lived up to the set expectations.
Also the latest developments are aiming at the reduction of the emitter doping quantity and, thus, the improvement of recovery behaviour. [132], [291]. Further progress can be made by reducing the depth of penetration.
However, with a dI/dt-rate of more than 1000 A/µs, some diodes with reduced p-doping do not show sufficient dynamic ruggedness. Figure 1.33 shows a failure statistics considering more than 16 production lots with 25642 free-wheeling diodes altogether. The failure results in a hole within the active area of the diode. This points to filamentation.
According to statistics, the number of failures caused by low-doped diodes and therefore higher resistance in the p-zone (Figure 1.33, 160 Ω/squ) was higher than that of diodes with re-increased doping (Figure 1.33, 60 Ω/squ), but those had shown impaired soft switching behaviour. This demonstrates the contrast of both requirements to this technology: soft switching behaviour on the one hand, and dynamic robustness on the other hand. Even accepting the restriction of soft switching behaviour could not completely avoid failures. In order to guarantee safe field application, all modules had to be subjected to a full load test in a chopper circuit under field conditions.

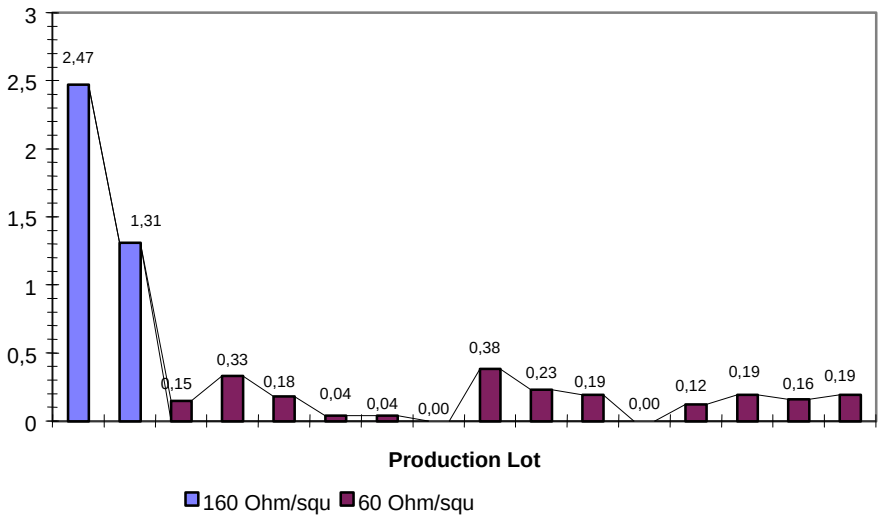


Figure 1.33 Proportion of failures of diodes with reduced p-doping for several production lots (at very high dI/dt)

It seems possible that the failures in Figure 1.33 may be reduced by technological optimization. However, it remains doubtful whether they can be completely avoided.
SEMIKRON has, at least, stopped any developments related to the emitter conception for free-wheeling diodes in fast switches.

1.3.4.2 Controlled Axial Lifetime (CAL) - conception

Recombination centre profiles similar to those shown in Figure 1.34a and 1.34b can be generated by implantation of protons or He^{++}-ions in silicon. Some time ago, this technology which required accelerators performing up to 10 MeV, had been exclusively reserved for research purposes, but the situation has changed. Basic research is interested more and more in the GeV-range, and medium energy accelerators are available for other fields of application.

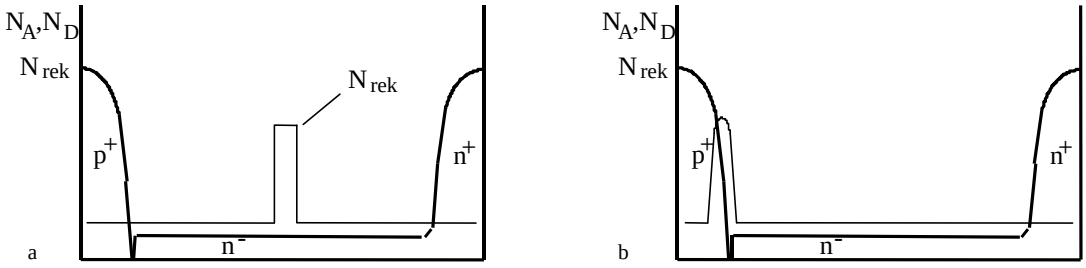


Figure 1.34 Axial profile of recombination centres generated by light ion radiation
a) Narrow partial zone with higher concentration of recombination centres in the middle of the n^--zone
b) Narrow zone with high concentration at pn-junction

The first assumption, that the best results could be achieved by implantation of a zone of highly concentrated recombination centres in the middle of the n^--zone as depicted in Figure 1.34a, had proven wrong. The arrangement of such a zone at the pn-junction as in Figure 1.34b turned out to be more favourable [292] [293].

Reference [147] explains that the relation between peak reverse current and forward on-state voltage is improved with approximation of the recombination centre peak to the pn-junction.

If the recombination centre peaks are arranged directly at the pn-junction, the charge carrier distribution will be inverted during on-state. The charge carrier distribution shown in Figure 1.31 results from a calculation based on the recombination centre profile according to Figure 1.35.

As for the CAL-diode, the recombination center peak (generated by He^{++}-implantation) has been arranged in the p-zone close to the pn-junction as in Figure 1.35, since this will lead to reduction of leakage currents. He^{++}-implantation has been combined with an adjustment of the basic charge carrier lifetime, preferably achieved by electron beam radiation.

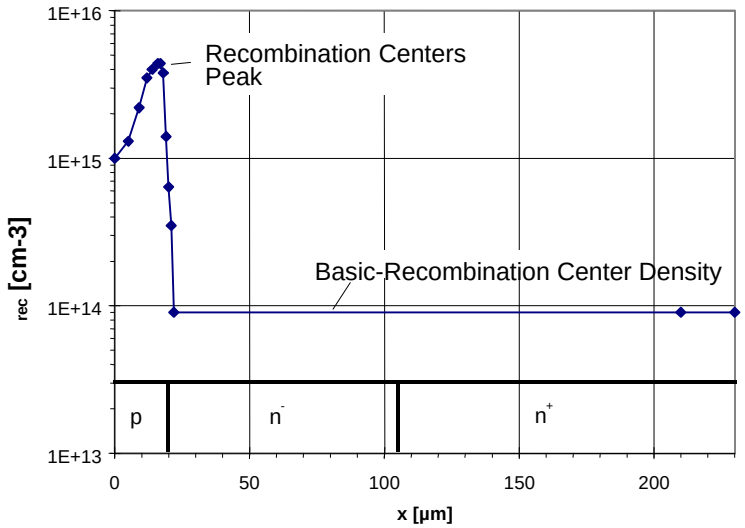


Figure 1.35 Recombination centre profile in the CAL-diode (scheme)

The characteristics of a CAL-diode in combination with an IGBT have already been referred to in Figure 1.24. The reverse peak current can be decreased by the recombination centre peak level, which is to be adjusted by the He^{++}-implantation dose. The biggest share of the storage charge of the CAL-diode occurs in the tail current, which, on the other hand, can be controlled by the basic recombination centre density. Reduction of the basic charge carrier lifetime will reduce tail current duration, however at increase of the on-state voltage of the diode. Recovery behaviour can be greatly controlled by both parameters, basic charge carrier lifetime and He^{++}-implantation dose. So the diode will show soft-recovery behaviour under any operating conditions, especially when low currents are applied.

CAL-diodes manufactured this way are proving a high **dynamic ruggedness**. CAL-diodes dimensioned for 1200 V and 1700 V have been tested under lab conditions at dI/dts up to 15 kA/cm²µs without destruction of the diode.

CAL-diodes are especially not likely to fail under the operating conditions shown in Figure 1.33. This fact is based on the production of over 26 million CAL-diodes up to now.

A ruggedness test of a 3,3 kV CAL-diode is shown in Figure 1.36. In the measurements in Figure 1.35 stress on the diode is still intensified by an additional parasitic inductance of 0.5 µH, generating a peak voltage of 1500 V directly subsequent to the commutation.

In contrast to other diodes, CAL-diodes may also be operated in this voltage range at a high dI/dt (here 2000 A/cm²µs).

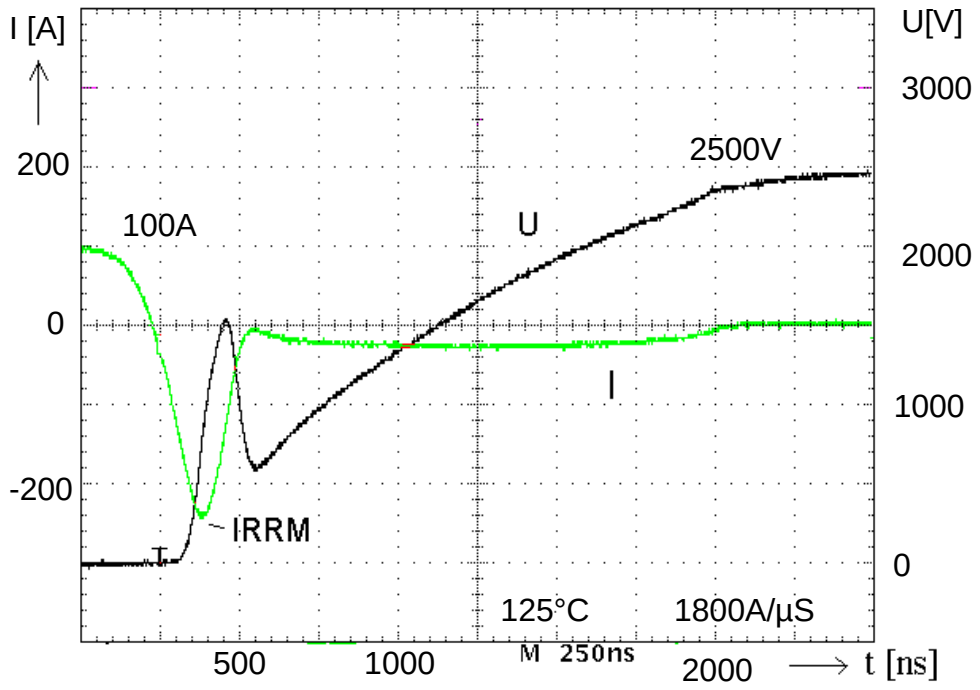


Figure 1.36 Ruggedness test of a 3300 V-CAL-diode

The base width w_B can be dimensioned comparatively narrowly for CAL-diodes, similar to the PT-dimensioning indicated in equations 1.10 and 1.11. This provides for a comparatively low on-state voltage or a better compromise between switching behaviour and on-state voltage, respectively. The base width is also of special importance to the turn-on behaviour of the diode. The forward recovery voltage V_{FR} increases proportionally to $w_{B;}$ components designed for 1700V and more are likely to generate some 100 V V_{FR} in the free-wheeling diode due to high dI/dt during turn-off of the IGBT. In contrast to conventional diodes, V_{FR} can be reduced by more than 50 % in 1700 V-CAL-diodes. [106].

Recently developed free-wheeling diodes for IGCTs as well as snubber-diodes [294] are being produced according to the CAL-conception, because

1. dynamic robustness is one of the most important demands,
2. dimensioning similar to PT-dimensioning results in an improved cosmic ray stability,
3. a favourable trade-off between on-state voltage and switching characteristics of the diode may be adjusted by the measure mentioned above,
4. minimum V_{FR} can be achieved in snubber-diodes,
5. a low leakage current can be realized compared to the conventional gold-diffusion process.

1.3.4.3 The concept of hybrid diodes

The concept of the hybrid diode was invented in 1991 [295], [296]. This conception is based on the idea that a soft-recovery diode is connected in parallel to a PT-diode with a low on-state voltage, but a snappy recovery behaviour, as shown in Figure 1.37.

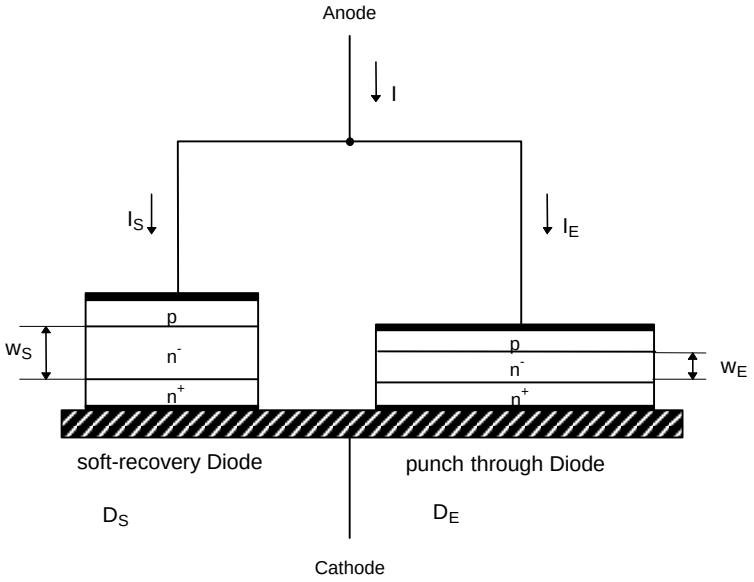


Figure 1.37 Structure of a hybrid diode

The function principle is shown in Figure 1.38. The main part of the on-state current is conducted by the snappy diode D_E. The rest is conducted by diode D_S. Current I_S is conducted through diode D_S and is the first to drop to zero passage, reaching its reverse current peak at t_1. At this time, diode D_E is still carrying forward current. At t_1 the pn-junction of diode D_S is free of charge carriers. Now, diode D_E is commutated with increased dI/dt. The total current is still determined by the outer circuit.

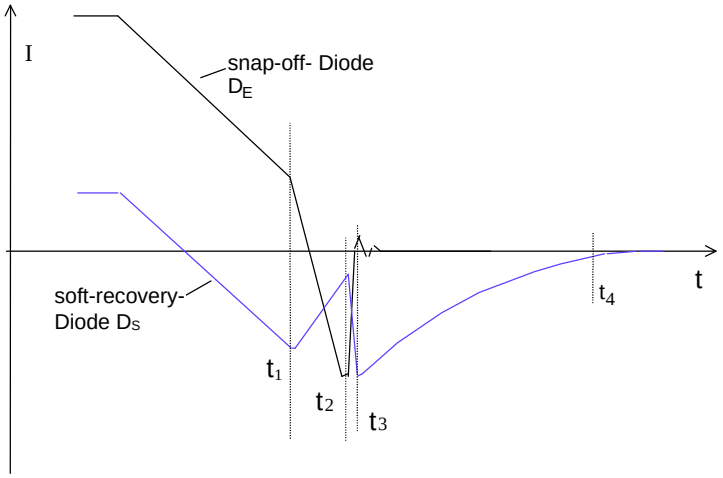


Figure 1.38 Current flow in the components of a hybrid diode

At t_2 the pn-junction of D_E is free of charge carriers. Between t_2 and t_3 the reverse current in D_E will snap off. It will then rise accordingly in diode D_S, which is not completely free of charge at that moment. The total current does not show a reverse current snap-off. Consequently, there will be no induced overvoltage. The charge carrier density in diode D_S is reduced between t_3 and t_4. The combination behaves soft.
To achieve efficient function of the hybrid diode, D_S has to supply sufficient charge even after the reverse current snap-off of D_E. To manage this, the soft diode D_S has to take on between 10 % and 25 % of the forward current. Therefore, the forward voltages have to be attuned.

The first modules that contained hybrid diodes were introduced to the market the beginning of 1996. They have been applied preferably as free-wheeling diodes in chopper circuits with 100V- or 200V-MOSFET switches. Here, an epitaxial diode designed for 400V is used as snappy diode D_E. The part of the soft-recovery diode D_S is taken over by a modified CAL-diode. The basic recombination centre density in it is kept on low-level, which results in a forward voltage of about 1.1 V at 150 A/cm².

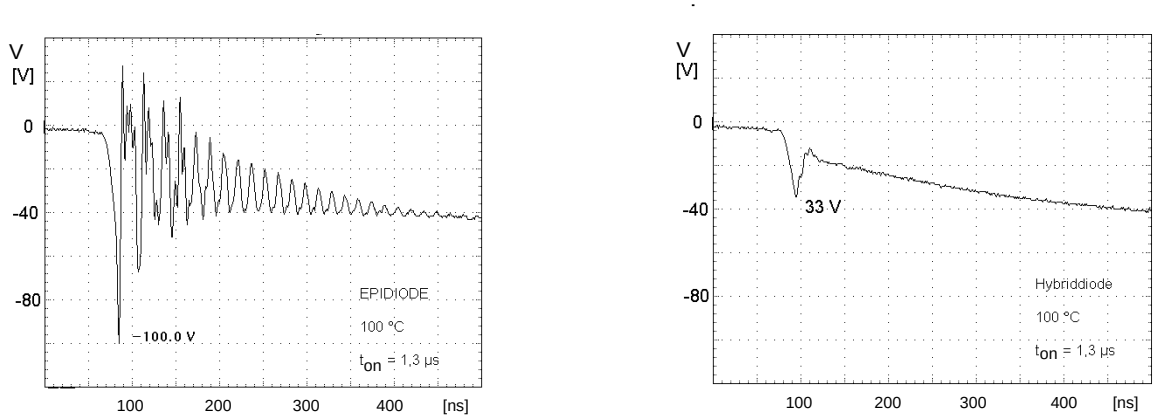


Figure 1.39 Voltage characteristic in a 350 A, 100 V chopper module,
on the left: with epitaxial diodes, on the right: with a hybrid diode

Figure 1.39 shows the voltage taken at turn-on of the MOSFET in a 350 A/100 V chopper module.

The diagram to the left shows the voltage characteristic for the free-wheeling diode being realized by parallelling of 7 epitaxial diodes.

The diagram to the right shows the voltage characteristic, if one of the 7 epitaxial diodes has been replaced by the soft-recovery diode D_S. The induced peak voltage will decrease from 100 V to 33 V, the interfering oscillations will disappear. By application of a like free-wheeling diode, the MOSFET can be turned on with a high dI/dt. If the turn-on time of the MOSFET is reduced from 1.3 µs to 0.3 µs by decreasing the gate resistance, the voltage characteristic will still be acceptable. Total losses of the circuit will drop to 48 % (= sum of line- and switching losses of all components).

Hybrid diodes are of special advantage in a voltage range of ≤ 600 V. In this range, diodes with a minimum w_B may be applied, if they are integrated as part of a hybrid diode. On the other hand, hybrid diodes will not offer decisive advantages to high-voltage applications, since differences in w_B between soft-recovery CAL-diodes and PT-diodes are not that serious.

1.3.5 Series and parallel connection of fast power diodes

1.3.5.1 Series connection

In series connections, attention must be paid to the symmetry of circuits with respect to static reverse voltage and with respect to the dynamic reverse voltage.

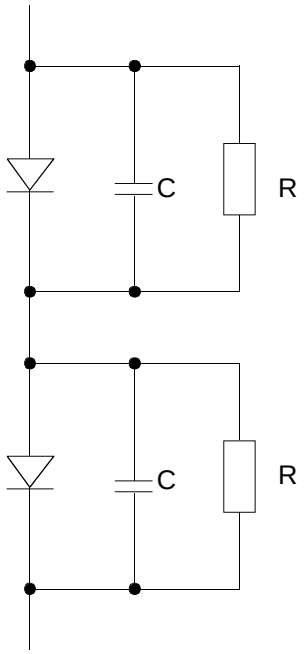


Figure 1.40 RC-circuit for series connection of fast diodes

With reference to the **static** reverse voltage, the variation of leakage current due to production processes will drive the components with the lowest leakage current to avalanche mode. As long as the avalanche stability of the components can be relied on, no resistors will have to be connected. If, however, components with a blocking capability of > 1200 V are connected in series, it is common practice to parallel a resistor.
This parallel resistor has to be dimensioned with respect to the fact that voltage distribution is always determined by its resistance.
If the leakage current is supposed to be independent of the voltage and if resistance tolerances are neglected, the simplified rule for dimensioning the resistance for series connection of n diodes of a specified reverse voltage V_r will be [297] :

$$R < \frac{nV_r - V_m}{(n-1)\cdot \Delta I_r} \qquad (1.15)$$

V_m stands for the maximum series voltage and ΔI_r for the maximum spread of leakage current in the diode, based on the maximum operating temperature. According to [297] it may be supposed with high confidence that

$$\Delta I_r = 0.85\ I_{rm,} \qquad (1.16)$$

with I_{rm} being specified by the manufacturer. According to this estimation, the current conducted through the resistor is approximately 6-times the leakage current in the diode.
Considering existing experiences, it will be sufficient for modern free-wheeling diodes to dimension the resistor in such a way that it will carry a current three times as high as the maximum leakage current of the diode. However, even then considerable power losses are generated within the resistor.

Dynamic voltage distribution may differ basically from static voltage distribution. If the pn-junction in one diode is free of charge carriers earlier than in another one, this diode will also take on voltage earlier.
If capacitor tolerances are neglected, a simple dimensioning rule can be used for this capacitor paralleled to a series connection of n diodes of a specified reverse voltage V_r:

$$C > \frac{(n-1)\cdot \Delta Q_{RR}}{n\cdot V_r - V_m} \qquad (1.17)$$

ΔQ_{RR} stands for the maximum variation of storage charge of the diodes. In all probability, it can be supposed that

$$\Delta Q_{RR} = 0.3 Q_{RR} \qquad (1.18)$$

if all diodes used are taken from the same production lot. Q_{RR} is specified by the semiconductor manufacturer. The charge stored in this capacitance is maintained in addition to the storage charge generated when the free-wheeling diode is turned off and has also to be taken up by the IGBT during turn-on. Based on these dimensioning rules, the occuring charge will be up to twice the storage charge of a single diode.

Free-wheeling diodes are usually not connected in series, due to the following additional sources of power dissipation:
- n-fold diffusion voltage of the pn-junction,
- power losses in the parallel resistor,
- increased storage charge to be taken up by the IGBT,
- more components necessary for the RC-circuit.

This holds, if a freewheeling diode for the required voltage range is available.
Series connection may however be made exceptionally, if the on-state power losses are not of considerable importance and if the application is dependent on short switching times and low storage charge, which is typical for low-voltage diodes.

1.3.5.2 Connection in parallel

Connection in parallel does not require any additional RC-circuit. It is important for parallel connection that the variation of the on-state voltage is kept as low as possible.

A decisive parameter to assess the parallelling capability is the temperature dependency of the on-state voltage. If the on-state voltage drops due to increasing temperature, the temperature dependency of the on-state voltage will be negative, the only advantage of which can be noticed in the power loss balance.
If the on-state voltage rises due to increasing temperature, the temperature dependency will be positive.

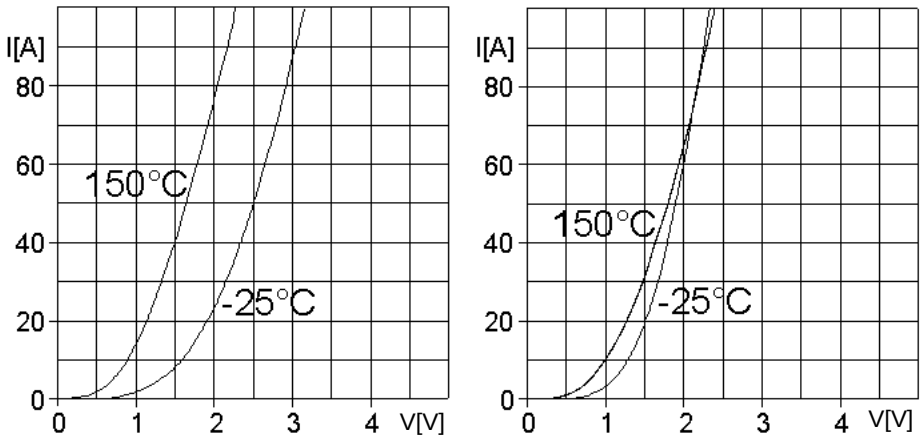


Figure 1.41 Temperature dependency of the forward on-state voltage for different types of diodes
Left side: extremely negative temperature dependency
Right side: positive temperature dependency above rated current (75 A)

A positive temperature dependency is of advantage for the application-specific parallelling, since a heated diode carries less current and the system stabilizes. An extremely negative temperature coefficient (> 2 mV/K) involves the risk of thermal instability for parallel connection of diodes, which always show spreading of the forward on-state voltage due to production processes.
Parallelled diodes are thermally coupled

- via the substrate in case of parallelling within the module,
- normally via the heatsink in case of parallelling of modules.

Principally, at a slightly negative temperature coefficient, this coupling effect will be sufficient to avoid thermal runaway of the diode with minimum on-state voltage. For diodes with a negative temperature coefficient of > 2 mV/K we recommend selecting a lower total rating than the current of the single diodes would add up to (derating).

1.4 Power modules: special features of multi-chip structures

1.4.1 Structure of power modules

In a power module *several power semiconductors* (MOSFET or IGBT chips and diode chips) which are *electrically isolated* from the mounting surface (heatsink) are integrated into a case on a common base plate.
The chips are soldered (or glued) to the metallized surface of an *isolation substrate*, which electrically isolates the chips from the module base plate, and at the same time creates good thermal conductivity.
The chip top sides are connected to the structured areas of the metallized surface by thin Al-bond wires.
In addition to that, passive elements such as gate resistors, shunts/ current sensors or temperature sensors (e.g. PTC-resistors) may be integrated into the module (hybrid) and also partly into the transistor chips (monolithic).
Moreover, “intelligent” power modules contain additional protection and driver circuits, see chapter 1.6.

The currently used isolation substrates for power modules are listed in the table below:

Isolation material

ceramic:	aluminum oxide Al_2O_3 aluminum nitride AlN (beryllia oxide BeO) (silicon carbide Si_3N_4)	*organic:*	epoxy polyimide (Kapton)

Substrates

Metal sheets:	(**D**irect **C**opper **B**onding) AMB (**A**ctive **M**etal **B**razing)	*Metal sheets:*	IMS (**I**nsulated **M**etal **S**ubstrate) Multilayer-IMS
Thick film layers:	TFC (**T**hick **F**ilm **C**opper)		

*DCB (**D**irect **C**opper **B**onding)*

Figure 1.42 shows the structure of a power module with IGBTs and free-wheeling diodes in the most common current technology with substrates made of *DCB*-ceramics with Al_2O_3 or AlN isolation, combining good thermal conductivity and high isolation voltage.

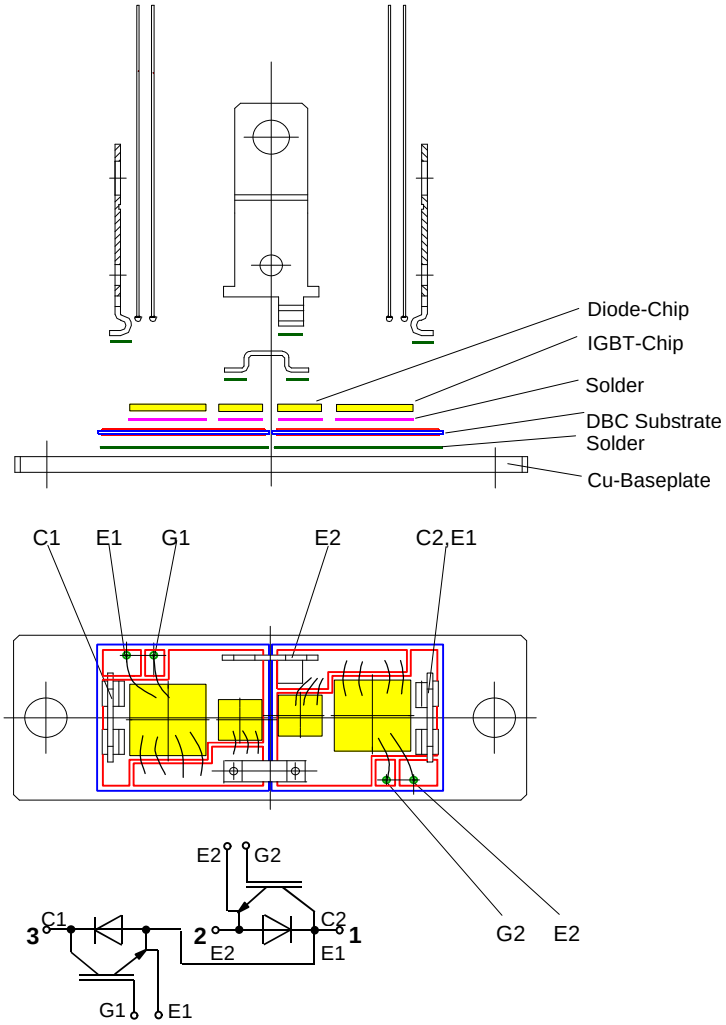


Figure 1.42 Structure of an IGBT module SKM100GB123D in a SEMITRANS 2 case

For production of a DCB-substrate, copper surfaces with a thickness of e.g. 300 µm are applied to the top and bottom areas of the isolation material (thickness 0.38...0.63 mm) by means of eutectic melting over 1000°C. After the necessary track structure for the module circuitry has been etched into the top side copper surface, the chips are soldered on, and the connection to the contacts on the chip top side is effected by bonding. The bottom side of the DCB-ceramic substrate is fixed to the module base plate (thickness e.g. 3 mm) mainly by soldering, see Figure 1.42.
Other module types (e.g. SEMITOP, SKiiPPACK, MiniSKiiP) do not necessarily require a base plate and the previous soldering procedure may be avoided. In these modules, the DCB-substrate is pressed on to the heatsink by means of suitable case constructions (see chapter 1.5).

Advantages of the DCB-technology compared to other structures are mainly the high current conductivity due to the copper thickness, good cooling features due to the ceramic material, the high adhesive strength of copper to the ceramic (reliability) and the optimal thermal conductivity of the ceramic material [52].

*AMB (**A**ctive **M**etal **B**razing)*

The AMB process (“brazing” of metal foil to substrate) has been developed on the basis of DCB technology. The advantages of AMB-substrates with AlN-ceramic materials compared to

substrates with Al_2O_3-ceramic materials are e.g. lower thermal resistance, lower coefficient of expansion and improved partial discharge capability.
Figure 1.43 explains the differences between DCB and AMB.

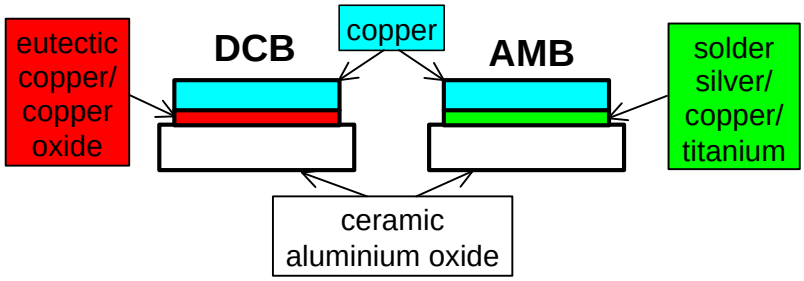


Figure 1.43 Direct Copper Bonding (DCB) and Active Metal Brazing (AMB)

*IMS (**I**nsulated **M**etal **S**ubstrate)*

IMS is mainly applied in the low cost/ low power range and is characterized by direct connection of the isolation material to the module base plate. For insulation, polymers (such as epoxies, polyamides) are usually applied to an aluminum base plate. The upper copper layer is produced in foil form and glued on the isolation substrate (similar to PCB production) and is structured by etching (Figure 1.44).

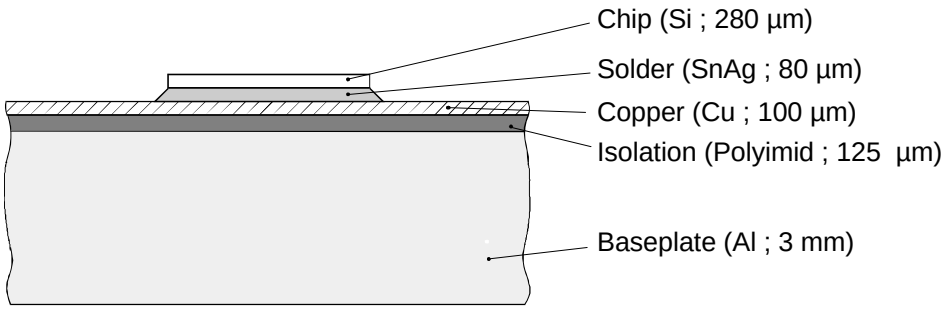


Figure 1.44 Basic structure of an IMS power module [194]

Advantages of IMS are low costs, filigree structure of tracks (possible integration of driver and protection facilities), high mechanical robustness of substrate and relatively wide substrate areas, compared to DCB.
The very thin isolation layer, however, leads to comparably high coupling capacitances against the mounting surface (see chapter 1.4.2.6). Furthermore, the thin upper copper layer only provides a comparably low spread of heat, which is improved by additional metallized heat spreading layers under the chips or by adding Al-particles to the isolation layer.

*TFC (**T**hick-**F**ilm-**C**opper)-thick film substrates*

Just as with DCB, the basic material for thick film substrates is an isolation ceramic, which is glued directly on to the base plate or a heatsink by means of silicone or applied by soldering (Figure 1.45).
The tracks on the top side of the ceramic substrate are made of copper and are applied by screen printing. The power semiconductor chips or other components are soldered or glued on to the tracks.

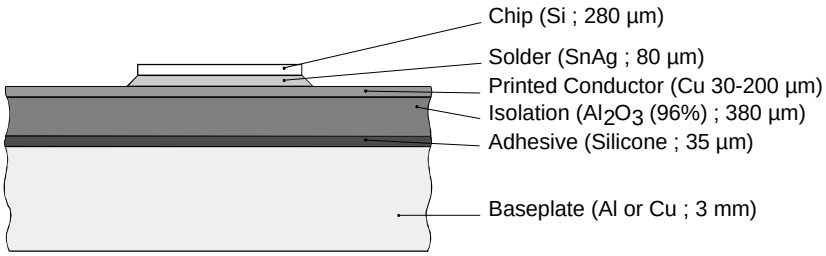


Figure 1.45 Basic structure of a TFC-power module [194]

TFC-technology can also be combined with standard thick film technology.
Since very low resistances may be produced by the paste materials which are usually applied in thick film technology, and since isolated tracks can be arranged one on top of the other and connected to each other, quite a number of system components may be integrated very closely together. However, the very filigree tracks (thickness e.g. 15 µm)will limit the current capability of such structures to about 10 A.

1.4.2 Features of power modules

The assessment of parameters relevant for module assemblies will always depend upon the specific application. The most important parameter with respect to railway drives, for example, will be reliability, whereas low costs are the decisive criterion for the production of consumer goods.
In this chapter, the applicability of a power module is to be regarded under the aspects of the following comprehensive criteria: "optimized" *complexity* of a module, *heat dissipation capability, isolation voltage and partial discharge stability, temperature resistivity and load-cycling capability of* the internal connections, *internal low-inductance structure, static and dynamic symmetry of the structure, electromagnetic stability, defined and safe failure behaviour, simple assembly and connection technology* and *favourable, non-polluting production and recyclability.*

1.4.2.1 Complexity

Optimized complexity cannot be defined in general. On the one hand, complex modules will reduce appliance costs and minimize problems encountered when several components are to be combined (parasitic inductances, interferences, wrong wiring).
On the other hand, increasing complexity will impair the universality of a module (reduced production lots). The number of tests and the costs per module will increase. With an increasing number of integrated components and connections the module will be more likely to fail and the efforts for repair will be higher. Drivers, sensors and protection facilities have to meet high demands for thermal and electromagnetic stability.

Up to now, none of the following module configurations has gained acceptance as a "world standard" with respect to the *integration of drivers*. The actual state of this development is described in chapter 1.6. The universality of power modules is greatly impaired by increasing the integration of driver functions, the module increasingly becomes a sub-system.
On the one hand, "intelligent" modules are aiming at real mass production markets (consumer, automotive), on the other hand markets are also involved, where many like applications can be supplied with innovative module systems consisting of similar basic elements. In spite of inevitable redundancies, the user may profit from reduced system costs due to the synergies achieved at the module manufacturer.
Regarding *the arrangement of IGBTs and diodes* in the most commonly used power modules, the configurations shown in Figure 1.46 have mainly gained a position in the market, meeting the

demands of most applications in power electronics and drive technology. Figure 1.46 is correspondingly applicable to modules with power MOSFETs, which are mainly applied in configurations for power supplies today.

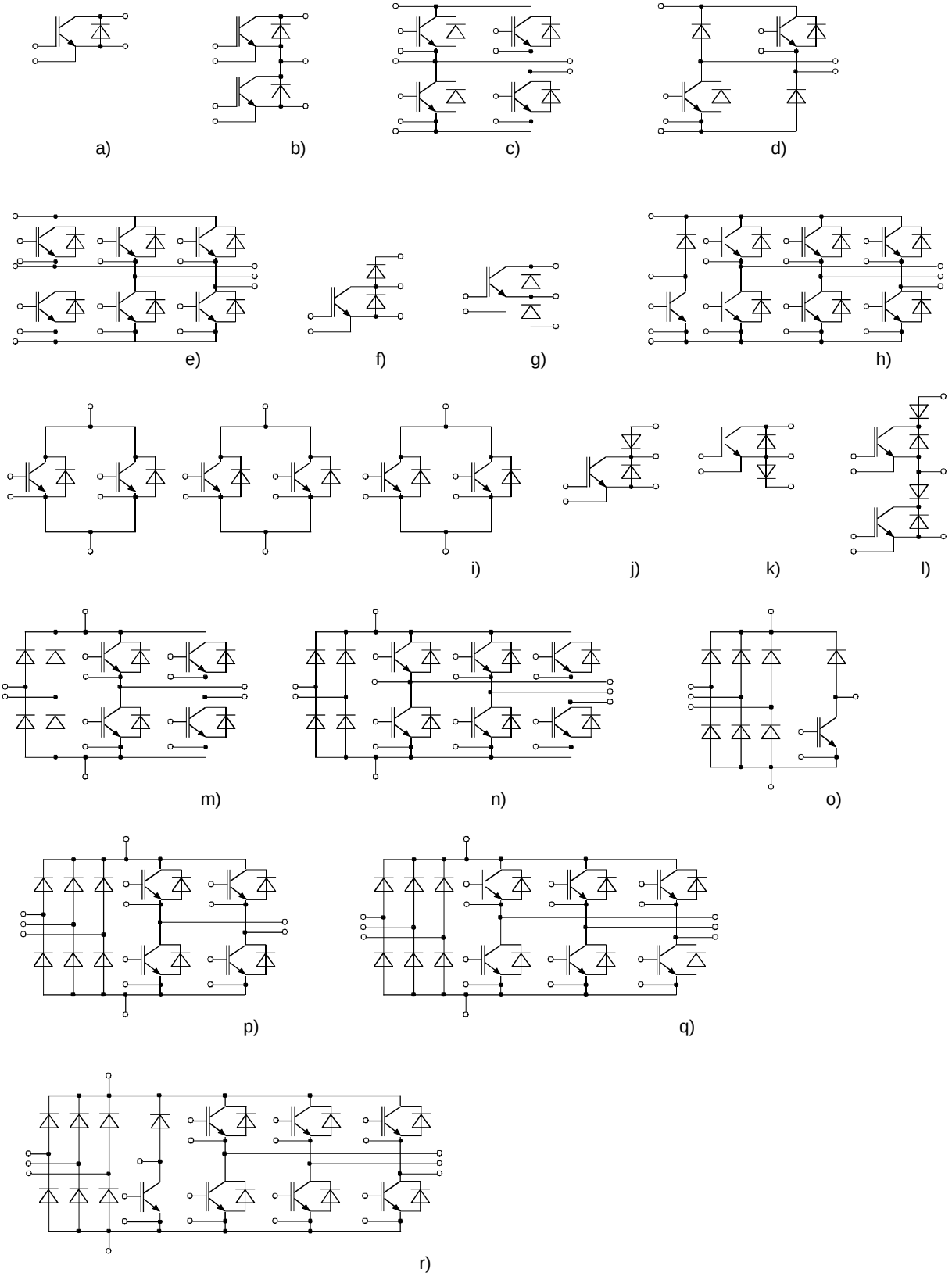


Figure 1.46 Important configurations of power modules with IGBTs and diodes

a) ...GA...: single switch, consisting of IGBT and hybrid inverse diode (as for MOSFET modules, here and in the other configurations, mostly just a parasitic inverse diode). In case of external bridge circuits, the inverse diodes are mutually acting as free-wheeling diodes.
b) ...GB...: dual module (halfbridge module) consisting of two IGBTs and hybrid diodes (free-wheeling diodes)
c) ...GH...: H-bridge with two arms consisting of IGBTs and free-wheeling diodes
d) ...GAH...: asymmetrical H-bridge with two diagonal IGBTs with hybrid inverse diodes (free-wheeling diodes) and two free-wheeling diodes across the other diagonal.
e) ...GD...: 3-phase bridge (Sixpack, inverter) with three arms consisting of IGBTs and free-wheeling diodes
f) ...GAL...: chopper module with IGBT, inverse diode + free-wheeling diode on the collector side
g) ...GAR...: chopper module with IGBT, inverse diode + free-wheeling diode on the emitter side
h) ...GDL...: 3-phase bridge “GD” with chopper “GAL” (brake chopper)
i) ...GT...: Tripack-module with three pairs of switches
j) ...GAX... single switch with series diode on the collector side (reverse blocking switch)
k) ...GAY... single switch with series diode on the emitter side (reverse blocking switch)
l) ...GBD... dual module with series diodes (reverse blocking switch)
m) ...B2U-diode rectifier and IGBT-H-bridge
n) ...B2U-diode rectifier and IGBT-inverter (three-phase-bridge)
o) ...B6U-diode rectifier and IGBT-chopper “GAL” (IGBT and free-wheeling diode on the collector side)
p) ...B6U-diode rectifier and IGBT-H-bridge
q) ...B6U-diode rectifier and IGBT-inverter (three-phase-bridge)
r) ...B6U-diode rectifier , IGBT-chopper “GAL” and IGBT-inverter (three-phase-bridge)

The SEMIKRON code designation system for SEMITRANS-IGBT and MOSFET modules is referred to in chapter 1.4.4; for SKiiPPACK, MiniSKiiP and SEMITOP see chapter 1.5.

1.4.2.2 Heat dissipation capability

In order to guarantee optimal utilization of the theoretical current capability, generated power losses have to be conducted safely and straightforwardly through the connection and isolation layers to the heatsink.

Figure 1.47 shows the internal characteristics of a module which affect the capability to dissipate heat (internal thermal resistance R/ internal thermal impedance Z), which determines the maximum losses in the module (current, switching frequency, voltage,...) together with cooling and ambient conditions.

The R-C elements shown in Figure 1.47, which are assigned to certain structural elements, are not meant to give an exact reflection of the physical heat conditions, but are only to illustrate the vertical flow of power and the temperature drop from the chip to the heatsink. The thermal resistances R_{th} characterize the static state, therefore they may be assigned to the structural elements.

However, capacitances replace physical elements, and may be gained by the transformation of real heat capacitances from volume elements (characterized by volume and specific heat) as opposed to a common thermal reference potential.

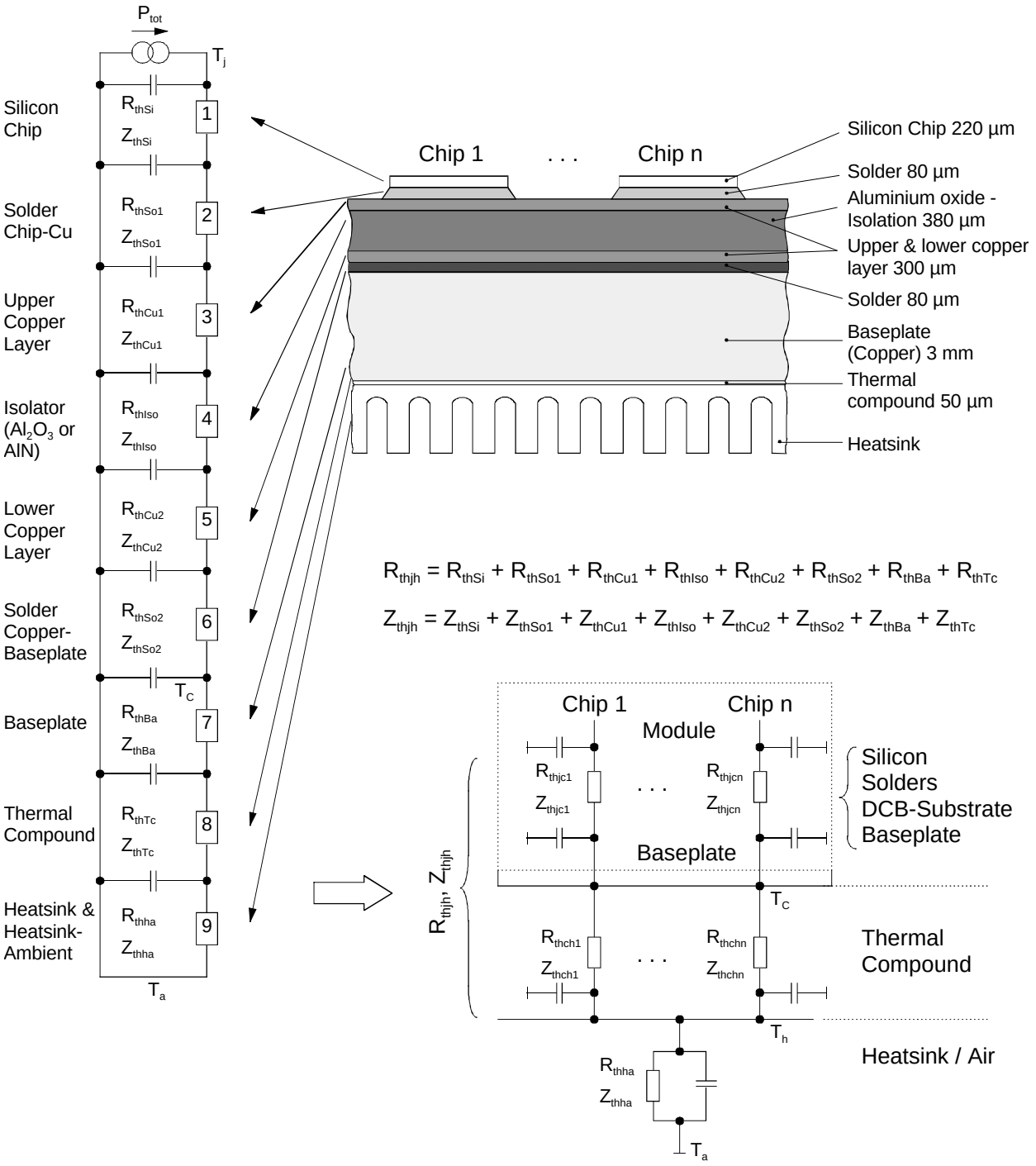


Figure 1.47a Basic structure of a power module with DCB illustrating the influences on heat dissipation

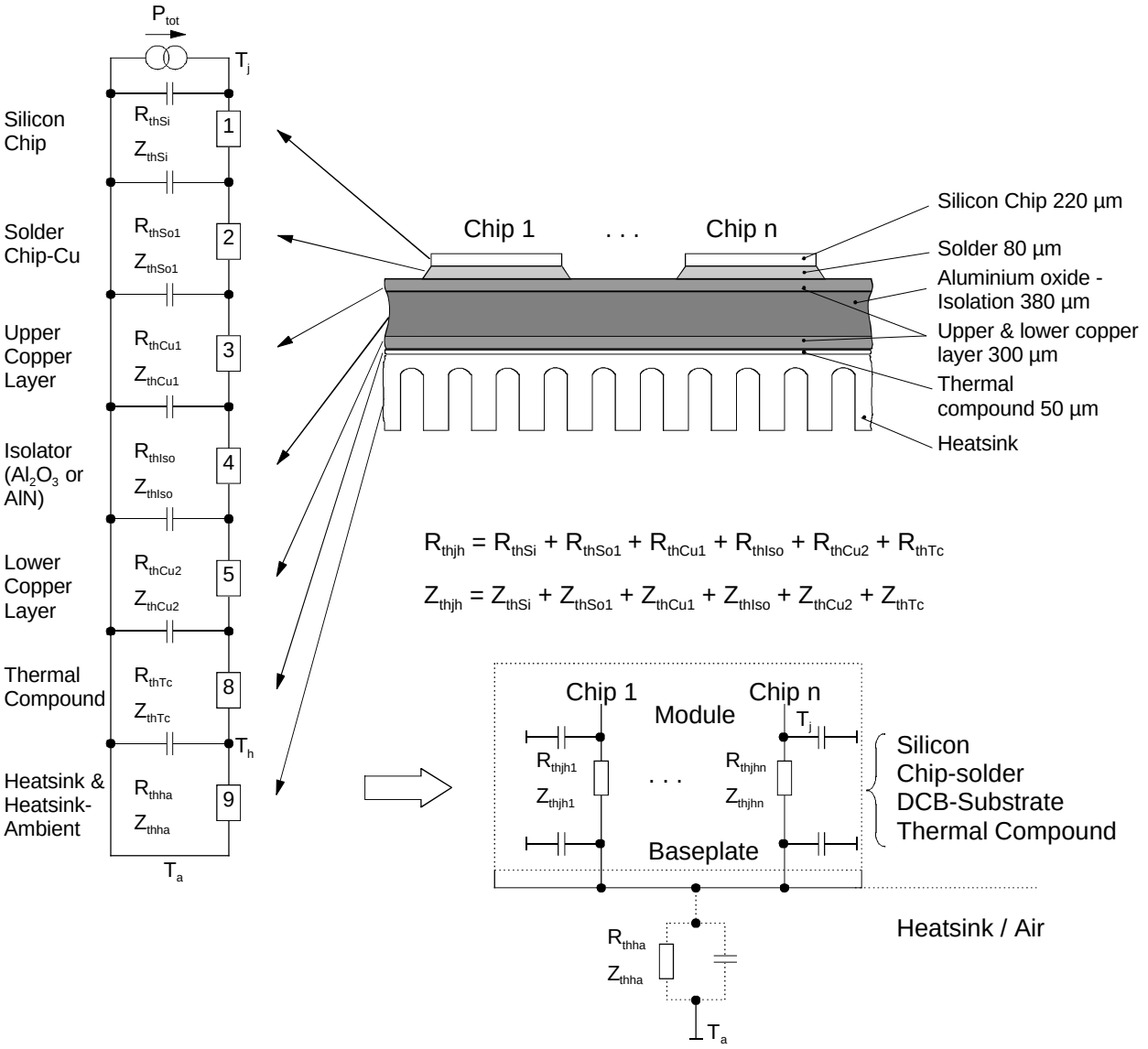


Figure 1.47b Basic structure of a power module with DCB without base plate illustrating the influences on heat dissipation

The quality of the dissipation of total power losses P_{tot} generated in chips during forward on-state and blocking state and during switching can be expressed by a minimized temperature drop

$\Delta T_{jh} = T_j - T_h$

from chip (chip temperature T_j) to heatsink (heatsink temperature T_h). It is quantified as thermal resistance R_{thjh} (stationary) or thermal impedance Z_{thjh} (transient).

Figures 1.47 and 1.48 illustrate the internal influences of the module on R_{thjh} and Z_{thjh}:
- chip (surface, thickness, geometry and position),
- structure of the DCB-substrate (material, thickness, top side structure),
- material and quality of connections between chip and substrate (solder, adhesive,..),
- existence of a base plate (material, geometry),
- backside soldering of the substrate to the base plate (material, quality),
- assembly of the module (surface qualities/ thermal contact to the heatsink, thickness and quality of thermal paste or thermal foil).

This list is still to be supplemented by the mutual heating of chips (thermal coupling) in complex power modules.

For modules with base plate the external thermal resistance or impedance (base plate-heatsink) is indicated with R_{thch} or Z_{thch}, respectively, in contrast to the "internal" resistance R_{thjc} or impedance Z_{thjc} (chip-base plate):

$R_{thjh} = R_{thjc} + R_{thch}$

$Z_{thjh} = Z_{thjc} + Z_{thch}$

This difference cannot be made for modules without base plate.

Figure 1.48 indicates the R_{thjc}-shares of the above-mentioned influences for the most common module structures of today described in chapter 1.4.2 with Al_2O_3-direct-copper-bonding (DCB)-substrates and Cu-base plates as well as for modules with insulated metal substrates (IMS).

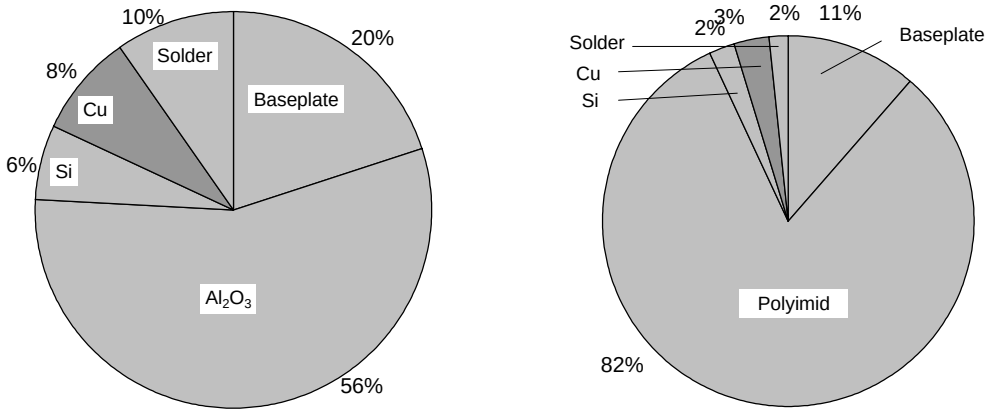


Figure 1.48 Influences on the internal thermal resistance of a 1200 V-power module, chip surface 9 mm * 9 mm [194]
a) For DCB-substrates (Al_2O_3) on a Cu-base plate
b) For IMS

The main share of thermal resistance is allotted to *internal module insulation* (the alternative of external insulation with foils or something similar would result in a deterioration of insulation by an even further 20 %...50 %!). Compared to Al_2O_3 with a purity of 96 % (heat conductivity $\lambda = 24$ W/m*K), which is applied as a standard in common DCB-modules, improvements can be made by using highly pure (99 %) Al_2O_3 ($\lambda = 28$ W/m*K) or aluminum nitride (AlN, $\lambda = 150$ W/m*K). In modules with high isolation voltages (thicker isolation ceramics) especially, AlN, which is still very expensive, is preferred nowadays.

Despite the high thermal conductivity of its material (Cu: $\lambda = 393$ W/m*K), the base plate also contributes to a considerable share of thermal module resistance due to its thickness (2.5...4.5 mm). This share may be only partly reduced, since a reduction of the base plate thickness would also bear the consequences of reduced temperature spreading and, thus, reduction of the area through which the heat passes under the chips. In modules without base plate the lack of heat spreading in Cu is compensated by missing thermal resistances of base plate and rear-side soldering.
Furthermore, on condition there is a suitable assembly technology (DCB is pressed on to the heatsink over wide areas), the chips will adhere closer to the substrate compared to constructions

with base plate, since base plate and heatsink will never fully contact each other because of unavoidable unevenness generated during the soldering process and, since the base plate is only fixed to the heatsink by means of pressure screws positioned at the margins (Figure 1.49).

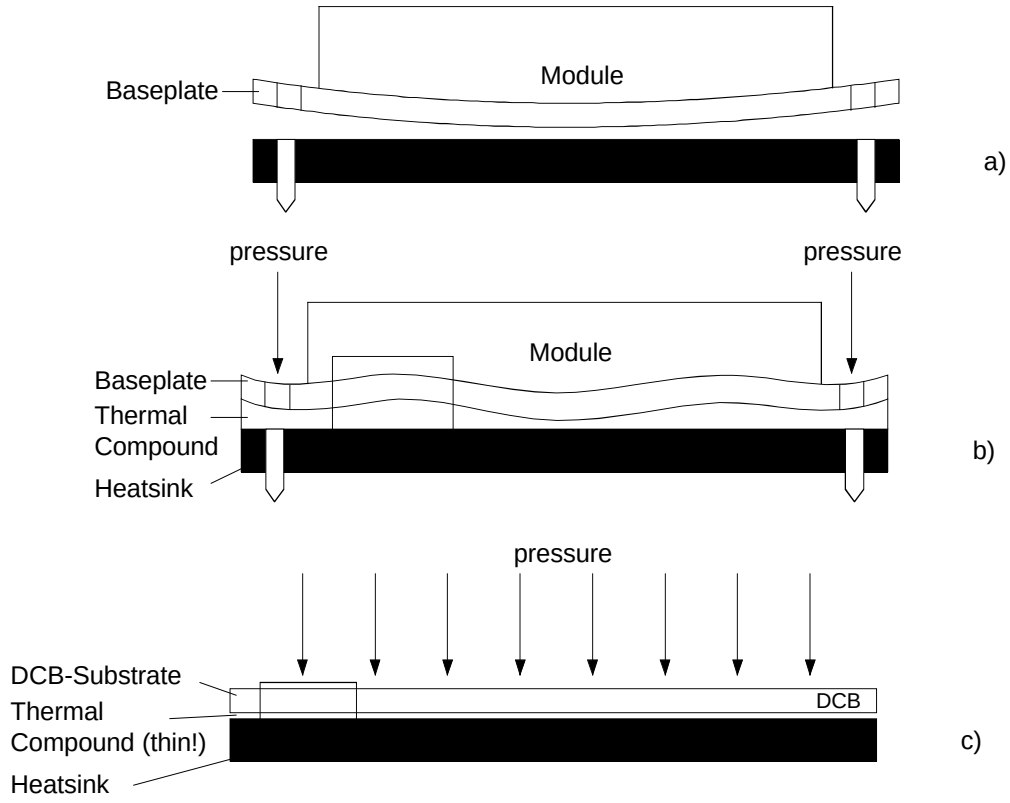


Figure 1.49 Problems arising through contact of power module to heatsink
a) Module with base plate before mounting (base plate with convex bending)
b) Module with base plate after mounting (strongly exaggerated!)
c) DCB-module without base plate (e.g. SEMITOP, SKiiP, MiniSKiiP)

Another factor that must not be neglected is the thermal resistance of the chip-substrate and (if applicable) substrate-base plate connections, which are produced as *solder connections* (e.g. λ = 75 W/m*K). The share of this resistance may be reduced by about 50 %, in cases where there is no base plate.

The thermal resistance share of *metal substrate areas* (Cu: λ = 393 W/m*K) depends mainly on the structure of the top side copper surface, which is used as chip carrier and internal electrical connection system of the module. While the lateral heat flow in the lower copper layer is practically not impaired, spreading of heat is limited by the geometrical dimensions of the copper layers under the chips. It had been determined in reference [194] that R_{thjc} of a chip of 6.5 mm*6.5 mm on a Al_2O_3-DCB-ceramic substrate exceeds the value of a ten times as big copper area by about 15 %, provided the chip and copper areas are identical.

The thermal resistance share of *silicon chips* increases proportionally to the *thickness of the chips*, which is determined by forward blocking voltage and chip technology.
Moreover, the *chip area* determines the area through which the heat passes between chip and base plate or heatsink.
On the one hand, the thermal resistance is reduced by increased chip areas due to a bigger area through which the heat passes. On the other hand, an increase of the area/ circumference ratio of

the chip will increase the influence of the thermal coupling of the heat flowing inside the chips on the thermal resistance, heat spreading will be diminished. Both opposite tendencies will lead to dependency of the thermal resistance R_{thjc} on the chip area A_{ch} shown in Figure 1.50.

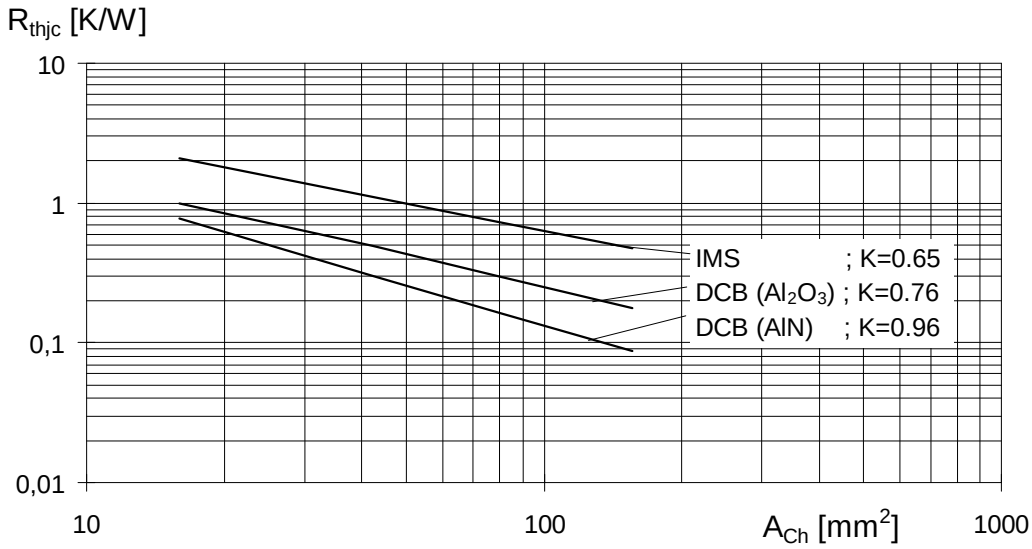


Figure 1.50 Dependency of thermal resistance R_{thjc} on chip area A_{ch} [194]

The dependency of R_{thjc} on A_{ch} is almost linear, when the total heat conductivity of the substrate (e.g. AlN-DCB) is high, since the chip area will hardly influence heat spreading. The worse the heat conductivity of the ceramics, the higher the non-linearity of the R_{thjc}-dependency on A_{ch}. Therefore, the maximum power loss density in the chips (chip utilization) will be drastically reduced by increasing the chip areas in like assemblies.

This correlation is also valid for the influence of module mounting to the heatsink, which is done with thermal paste or thermal foils. With a value of $\lambda = 0.8$ W/m*K the heat conductivity of this layer is relatively low, which will cause a thermal transient resistance R_{thch} between module base plate and heatsink. Besides the thickness d of the thermal paste layer, the R_{thch}-share in the thermal resistance R_{thjh} between chip and heatsink will also rise with increasing chip area.

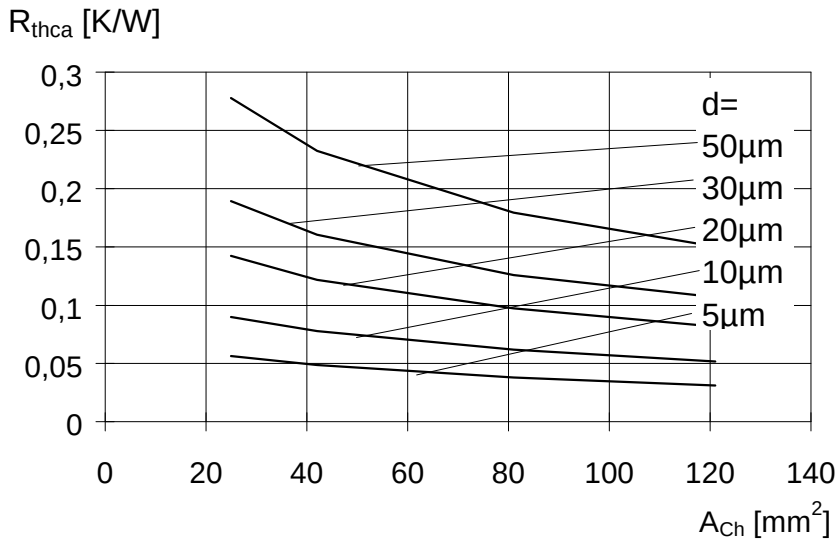


Figure 1.51 Thermal resistance of thermal paste R_{thca} of a DCB-substrate (Al_2O_3) according to [279] and [194]

First of all, Figure 1.51 shows the influence of an optimal mounting technology (thin thermal paste layer) on thermal parameters.
Secondly, it shows that thermal limits are set to the use of bigger chips to increase power output; the thermal resistance share R_{thjh} of thermal paste, for example, will amount to approximately 30 % at an application thickness of 30 µm for a 50A-IGBT-chip (9 mm * 9 mm).
Currently, the maximum chip sizes used in power modules are between 30 mm^2 (IMS) and 150 mm^2 (Al_2O_3-DCB). Higher power output can be reached by decentralization of heat sources (paralleling of a maximum number of chips).

For the sake of a small geometry of the modules, more or less intensive *thermal coupling* of chips has to be accepted, which is due to the tight arrangement of transistor and diode chips.
According to the calculations in reference [194] an increase of the chip temperature caused by thermal coupling e.g. on a Al_2O_3-DCB-ceramic substrate should always be taken into consideration, if the distance a of the chips equals:

$$a = 0.58 \cdot \sqrt{A_{Ch}}$$

As already mentioned above, apart from the static behaviour of power modules the *dynamic thermal behaviour*, which is characterized by the thermal impedance Z_{th}, is also of major importance.

Figure 1.52 shows the characteristic of the thermal impedances Z_{thjc} of a module with Al_2O_3-DCB-substrate for different chip areas versus time.

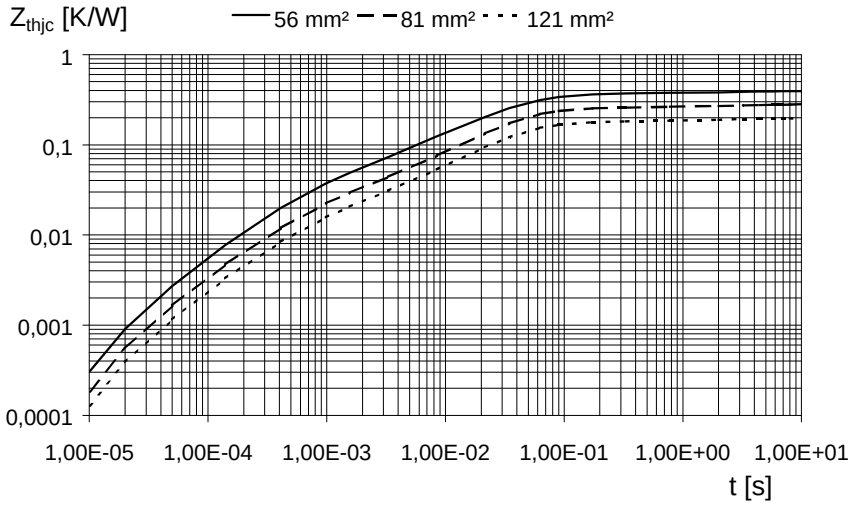


Figure 1.52 Thermal impedances Z_{thjc} of a module with Al_2O_3-DCB-substrate for different chip areas versus time [194]

For the given module structure the Z_{th}-characteristics for different chip areas may be shifted against each other, i.e. the absolute values will change proportionally to the chip area, however, without influencing the time constants of the exponential functions.
Accordingly, thermal impedances for different chip areas may be calculated similarly to the thermal resistances in a given structure by

$Z_{thjc1}(t)/Z_{thjc2}(t) = R_{thjc1}/R_{thjc2} = (A_{Ch2}/A_{Ch1})^K$.

Hereby, the exponent K, as a parameter indicating the influence of heat accumulation effect, may be determined from Figure 1.50 [194].

1.4.2.3 Isolation voltage/ partial discharge stability [275]

Advancing in the high-voltage application range will result in increasing demands on IGBT-modules for high isolation voltages and a high partial discharge stability.
Isolation and partial discharge stability are dependent on the thickness, material and homogeneity of the insulation on the chip bottom and the case materials and, sometimes, on the chip arrangement too.

The current transistor modules are subject to isolation test voltages between 2.5 kV_{eff} and 9 kV_{eff}, applied to every module during production.

Figure 1.53 shows the maximum attainable isolation voltages for different isolation substrates and today's standard substrate thicknesses d.

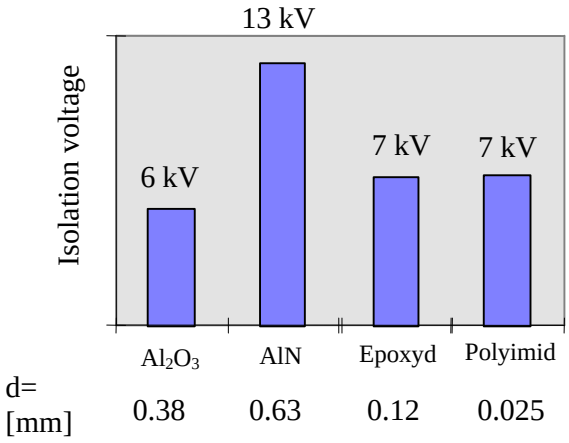


Figure 1.53 Isolation voltages for different isolation substrates with DCB, IMS and TFC

1.4.2.4 Power cycling capability

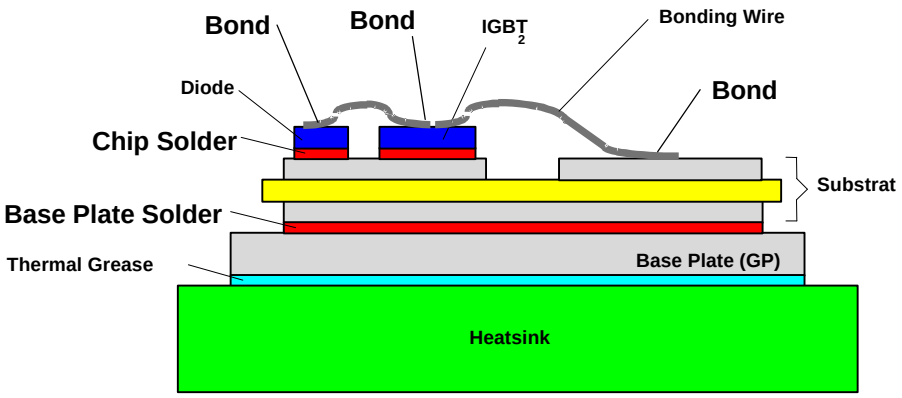
Power cycling at frequencies below approximately 3 kHz, especially at duty cycle operation, such as prevails in traction, lift and pulse applications, will expose the internal connections in a module to temperature cycling, such connections being:

- bonded joints,
- underside soldering of chips,
- solder connection of DCB and base plate,

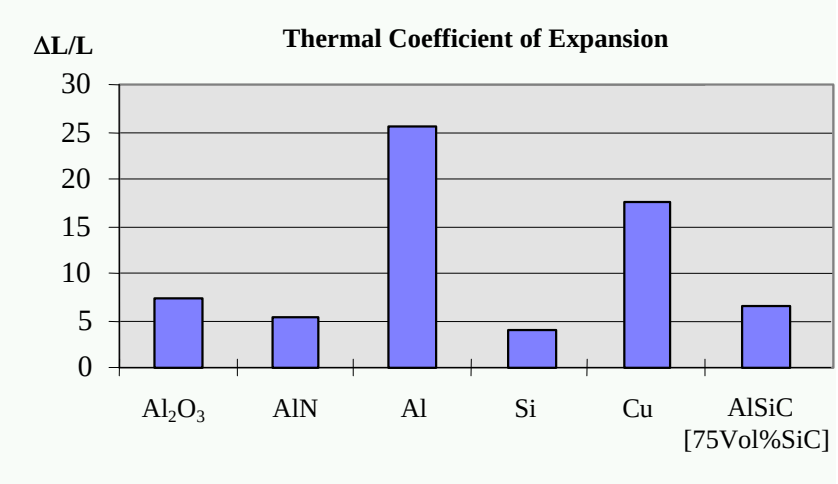
as well as substrate lamination (Cu on Al_2O_3 or AlN).
The different coefficients of the length expansion of the layers cause thermal stress during production and operation, which will finally lead to wear and tear of the material; module load life (number of possible switching cycles) will be shortened when the amplitude of the chip temperature fluctuation increases during these cycles.

Test procedures are dealt with in chapter 2.7; the correlation of module life and temperature cycling amplitude will be explained in chapter 3.2.3.

Figure 1.54a explains the structural details relevant to the module life of an IGBT.

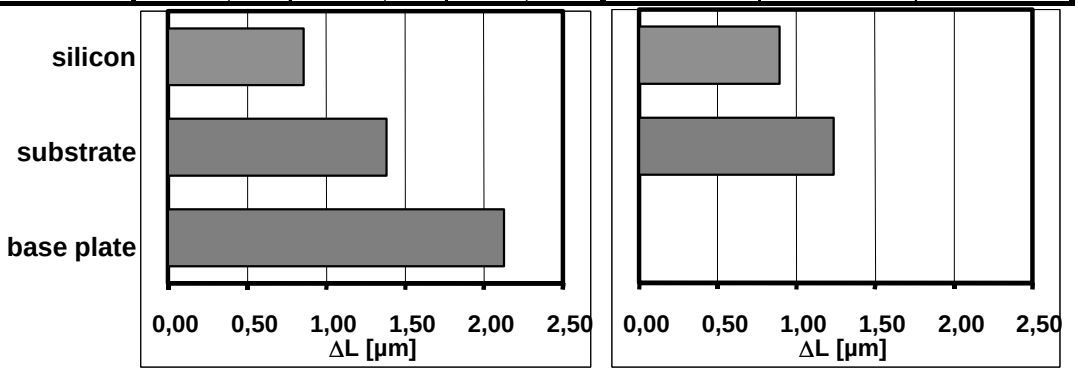


a)



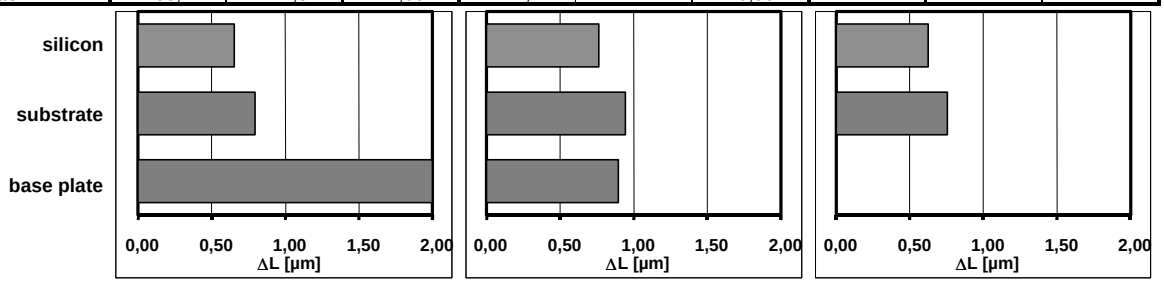
b)

System:	standard 34mm module 0,38mm-Al2O3 / Cu base plate			SKiiP pressure system 0,38mm-Al2O3		
Results:	T-Tkk [K]	ΔL/L [1E-6/K]	ΔL [µm]	T-Tkk [K]	ΔL/L [1E-6/K]	ΔL [µm]
silicon	69,7	4,1	0,86	62,6	4,1	0,77
substrate	55,4	8,3	1,38	48,3	7,8	1,13
base plate	40,5	17,5	2,13	—	—	—



c)

System:	standard 34mm module 0,63mm-AlN / Cu base plate			34mm module 0,63mm-AlN / AlSiC base plate			SKiiP pressure system 0,63mm-AlN		
Results:	T-Tkk [K]	ΔL/L [1E-6/K]	ΔL [µm]	T-Tkk [K]	ΔL/L [1E-6/K]	ΔL [µm]	T-Tkk [K]	ΔL/L [1E-6/K]	ΔL [µm]
silicon	53,4	4,1	0,66	61,8	4,1	0,76	50,8	4,1	0,62
substrate	46,6	5,7	0,80	55,2	5,7	0,94	44,2	5,7	0,76
base plate	38,1	17,5	2,00	42,7	7	0,90	—	—	—



d)

Figure 1.54 Thermal expansion in a power module
a) Standard assembly of module with base plate
b) Thermal coefficient of expansion
c) Comparison: assembly with and without copper base plate; Al_2O_3 – substrate
d) Comparison: assembly with and without copper/AlSiC base plate; AlN - substrate

Figure 1.54 makes clear that the *solder connection of the substrate to the copper base plate* is most critical, since it is the most extensive connection - medium differences in the expansion coefficients of the adjacent materials provided. Therefore, high-quality solders and sophisticated soldering procedures have to be applied in order to avoid deformation and destruction of the substrate also in case of high temperature cycling amplitudes.
Moreover, often the DCB-substrates are divided up to keep the absolute difference of the expansion coefficient as small as possible by reducing the solder areas.
Other, lately developed module types are replacing copper by a material with a smaller expansion coefficient (such as AlSiC), see chapter 1.5.4 and [206].

It is also shown in Figure 1.54 that modules with AlN-DCB are especially sensitive, because the expansion coefficient of AlN is very similar to that of the chip silicon, but there are greater deviations to copper than with Al_2O_3. Therefore, today's modules with AlN-DCB and Cu-base plate cannot completely utilize the actual material performance with reference to the corresponding datasheets.

It has become very obvious that one of the main causes for wear and tear can be eliminated by doing without a base plate and the necessary soldering, as long as the heat transfer from the substrate to the heatsink can be sufficiently ensured and the disadvantages of reduced heat spreading can be compensated. This has been realized with SKiiP, MiniSKiiP, SEMITOP and SKiM technologies (see chapter 1.5).

The temperature cycling capability of the *soldering of the chips to the substrate* can be improved by

- use of AlN-substrates with less deviation of the expansion coefficient to Si than Al_2O_3,
- substitution of soldering by low-temperature connections; the connection between chips and substrate is realized by sintering silver powder at comparably low temperatures (150...200°C), which will minimize thermal stress among the materials during production.

Bond connections. Also the lifetime of the connection between bond wire and chip is influenced decicively by the difference in thermal coefficients of expansion.
Silicon shows a relative slight lenght expansion (4.7 ppm/K) during power cycling. However, the Al-metallization of the emitter and gate contacts which are stressed by the same temperature fluctuations shows a considerable higher relative lenght expansion (23 ppm/K).
The stress inside of the metallization caused by this difference in expansion effects a rearrangement of the crystal grains. This process is called „reconstruction".
The reconstruction - mostly identifiable by an optical dispersive surface – leads to the destruction of the bond wire connection [304]. Reconstruction of Al-contact metallization can be reduced by a polyimide-cover.
The lifetime of the bond connection on the chip contact area is increased considerably using bond covers. However, another type of failure occurs. The mechanical deflection of the bond wire during thermal alternating stress caused by the different thermal expansion of substrate and Al-wire leads to a fracture of the bond wire nearby the „bond-heel" on the PCB-sided juncture since the chip-sided „bond-heel" is mechanical strengthened by the polyimide cover.
Bond wire failures are mostly observed in lifetime tests whereas the failure is caused really by ageing of the solder layer. Caused by growing cracks in solder layer the thermal resistance increases and effects a increasing chip temperature and thus a higher stress for both the bond connection and chip solder layer. Finally, this positive feedback leads to a failure.
In any case, the ageing of solder connection has to be investigated at failure analysis. Using today's technologies solder connections and bond connections have nearly the same lifetime at cycles with high temperature ripples ($\Delta T \approx 100K$).
In state-of-the-art power cycling test equipment forward voltage drop and thermal resistance of power devices are measured and recorded. So, both degeneration of solder layer and bond connection failures (steps in foward voltage drop characteristic) can be observed.

Bond connections in IGBT and diode-disc cells have been replaced by pressure contacts with a higher temperature cycling capability due to pressure contact technology. Processes for transferring this direct pressure contact technology to power modules are also currently being developed.

1.4.2.5 Internal low-inductive structure

With the example of a halfbridge module, Figure 1.55 shows the most important internal parasitic inductances of a module, resulting from the necessary connections among the chips and to the module terminals (bond wires, internal connections).

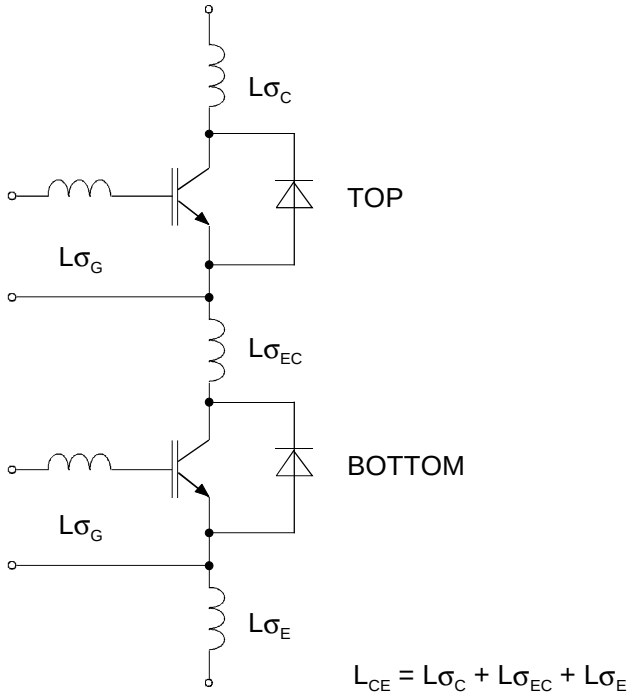


Figure 1.55 Parasitic inductances in a dual IGBT-module
$L_{\sigma G}$: parasitic gate inductances
$L_{\sigma C}$: parasitic TOP-collector inductance
$L_{\sigma EC}$: parasitic inductance between TOP-emitter and BOTTOM-collector
$L_{\sigma E}$: parasitic BOTTOM-emitter inductance
L_{CE}: total parasitic TOP-collector-BOTTOM-emitter inductance

Minimization of these inductances, which induce overvoltages during turn-off and cause a dI/dt reduction during turn-on as well as inductive coupling of control and power circuit, will directly affect the performance of power modules.
Moreover, parasitic inductances in modules with internally paralleled chips may cause unequal dynamic performance of the chips and oscillations between the chips.
Chapter 3.4.1 gives details on these correlations.

1.4.2.6 Internal structure-adapted to EMC

The short rates of rise of current and voltage within the ns-range realizable with MOSFET- and IGBT-modules generate electromagnetic interference with frequencies far beyond the MHz-range. Therefore, the parasitic elements typical of the internal and out-leading paths of propagation in the module exert considerable influence on the interference voltages generated.

Suitable isolation materials, small coupling areas or conductive shields can reduce, for example, asymmetrical interferences [193].

In addition to that, the internal connections in the module have to be of such a structure, that excludes failures caused by outer stray fields or transformatory couplings into control lines.

Another aspect of electromagnetic compatibility is the “earth current“, i.e. the current $i_E = C_E * dv_{CE}/dt$ that flows due to the capacitance C_E of the isolation substrate caused by the dv_{CE}/dt generated in the IGBTs during switching via the earthed heatsink to the earth connector.

This earth current is identified as earth-leakage current by line monitors; its permissible maximum value is to be limited to 0.1...5 % (1 % anticipated) of the nominal output current as soon as the new EN 50178 comes into effect.
Accordingly, the permissible switching speed will increase proportionally to the decrease of capacitance of the isolation substrate.

Figure 1.56 compares the capacitances of the most commonly used substrates with respect to their standard thicknesses. The deviating dielectric constants and the standard thicknesses depending on thermal conductivity (thickest substrate material is AlN with 630 µm, thinnest substrate is required in IMS-structures with 120 µm for epoxy isolation and 25 µm for polyimide isolation) result in respectively differing capacitances C_E and, thus, in different limits of the maximum switching velocity dv_{CE}/dt for the maximum tolerable earth current i_E.

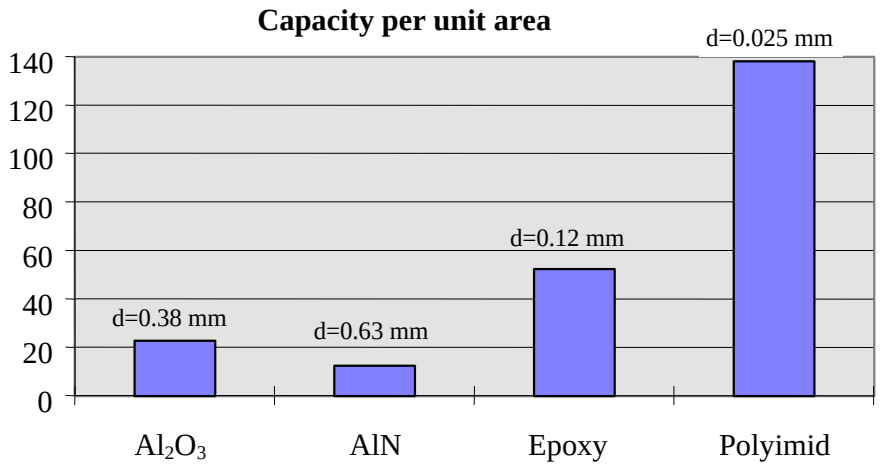


Figure 1.56 Capacitance per unit area for different isolation substrates

1.4.2.7 Defined safe behaviour in case of module failure

In the case of module failure (probably caused by use of wrong driver) the total energy stored in the DC-link capacitors will be transferred, for example, in a voltage-supplied circuit within the module case. After melting the bond wires this energy is mainly stored in the generated plasma, which allows the module to explode.
In conventional transistor modules this may cause circuit interruption, short-circuit of the main terminals or even bridging of the isolation; plasma and particles of the case might be spread over the module surroundings with high kinetic energy.
With the proper case construction, the dangers involved may be limited and the particles spread are guided in a defined direction.
The latest developments in this field guarantee, for example, that up to a defined energy level of e.g. 15 kJ no particles will leave the module; even at 20 kJ the case might break, but no solid metal particles would be hurled out [196].

1.4.2.8 Non-polluting recycling

Today's power modules usually exclude toxic materials (e.g. BeO) and the number of materials used is kept as low as possible.
Case and other materials are flame-resistant and must not release toxic gas during burn-out (UL-specification).

The module has to be split up as simply as possible in metal and non-metal components during recycling. Therefore, the currently available modules are cast solely with elastomeric materials (soft moulding).

1.4.3 Assembly and connection technology: types of cases

Cases of current power modules containing 1...7 MOSFET or IGBT-switches are mostly equipped with screw, plug-in or solder-terminals.
For the majority of transistor modules, different manufacturers are striving for a large degree of compatibility with partly historically developed structures (Figure 1.57).

First of all, the inevitably deviating high-integration modules (e.g. SKiiPPACK, MiniSKiiP) are not to be considered in the following.

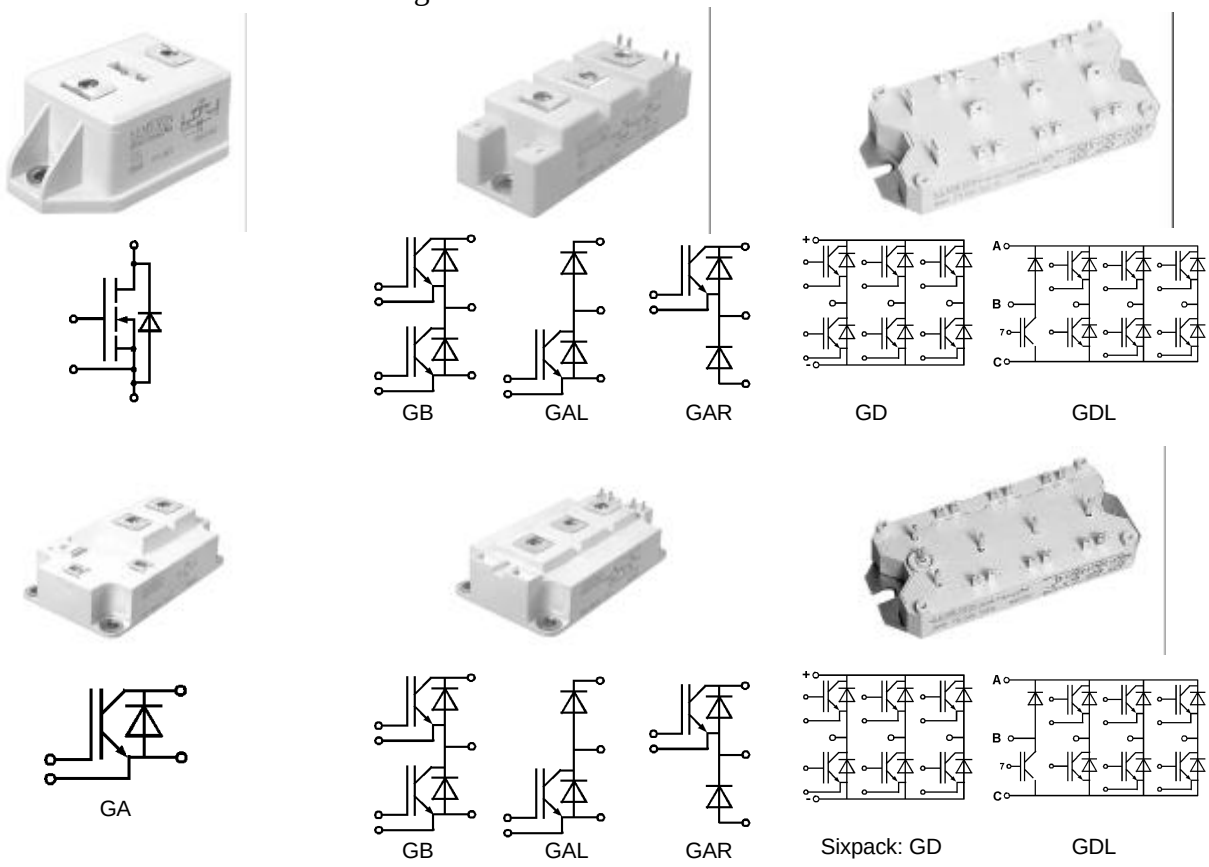
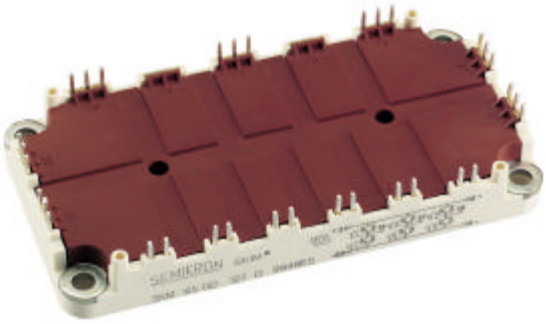
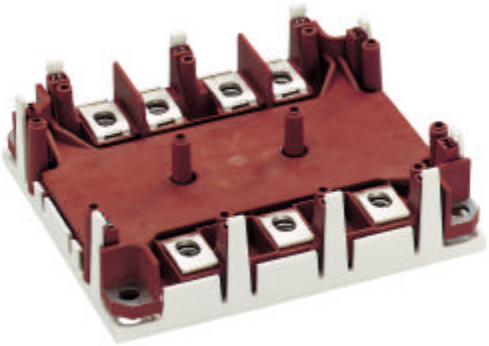


Figure 1.57a Transistor modules with base plate

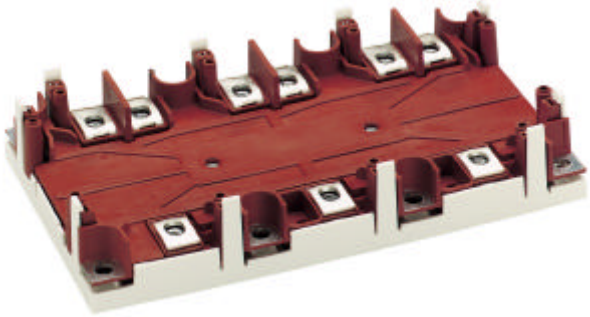
SEMITOP



SKiM 3



SKiM 4



SKiM 5

Figure 1.57b Transistor modules without base plate

The highest degree of standardization is assigned to module types with screw connectors. The main supplies may be contacted by busbars or sandwich assemblies. Often, additional outputs are provided for control and sense-units (e.g. control-emitter, sense-collector) in order to minimize the influence of inductive voltage drop in the main circuit generated during switching, especially at the bonded connecting wires. Auxiliary supplies are mostly designed as 2.8 mm flat strip plug connectors, sometimes also as screw connectors.
For low-current modules the use of 6.3 mm or 2.8 mm flat strip plug connectors for power and control circuit, respectively, has also been very common up to now.
Solderable modules for PCB-assembly (e.g. SEMITOP, ECONOPACK) are gaining importance, because they offer cost advantages during automatic production and tooling procedures. Optimized layout of connectors will take care of low-inductance assemblies, and currents up to 100 A may be realized by paralleling several solder connectors. In this respect, the necessary track sections (for high currents) and the realization of long creepage paths on the PCB might be problematic.

1.4.4 SEMIKRON code designation system for SEMITRANS- and SEMITOP-power modules

Different functions, internal circuits, current and voltage range and other informations are coded by the manufacturers in their type designations.
The following tables indicate the code designation system for SEMIKRON MOSFET and IGBT-modules.

SEMITRANS power-MOSFET-modules

There is an “old“ and a “new“ designation code for SEMITRANS-MOSFET-modules. The “old“ designation code had been introduced with the first MOSFET-modules, some of which are still being produced, at the end of the eighties following the PRO-ELECTRON-recommendations by SEMIKRON. All newly developed modules are designated according to the “new“ code, which gives more information and corresponds basically to the designation code for SEMITRANS-IGBT-modules.

“old” designation code, e.g.
SK M 1 5 1 A F R C

SEMIKRON component

MOS technology

Circuit configuration
1: Single switch
2: Dual mode (halfbridge)
3: Special type
4: 4-pack (H-bridge)
6: 6-pack (three-phase-bridge)

Voltage grade
0: V_{DS} = 50 V 5: V_{DS} = 500 V
1: V_{DS} = 100 V 8: V_{DS} = 800 V
2: V_{DS} = 200 V 9: V_{DS} = 1000 V
4: V_{DS} = 400 V

Internal arrangement
0: 4...5 chips in parallel
1: 6 chips in parallel
2: 2 chips in parallel
3: Special type
4: 4+4 chips

A: avalanche-proof single chips
F: built-in fast inverse diode
R: built-in gate series resistors
C: built-in gate driver circuit (manufactured until 1996)

“new” designation code, e.g.
SK M 120 B 020

SEMIKRON component

MOS technology

Drain current grade
(I_D/A at T_{case} = 25°C)

Circuit configuration
A: Single switch
B: Dual mode (halfbridge)
D: 6-pack (three-phase-bridge)
M: 2 MOSFETs in center tap connection

Drain-source voltage grade
(V_{DS}/V/10)

SEMITRANS IGBT-modules

z.B. **SK M 100 G B 12 3 D L**

SEMIKRON component

M: MOS technology
D: 7D-pack (B6-diode input bridge with IGBT chopper)

Collector current grade (I_C/A at T_{case} = 25°C)

G: IGBT switch

Circuit configuration
A: Single switch
AL: Chopper module (IGBT and free-wheeling diode on collector side)
AR: Chopper module (IGBT and free-wheeling diode on emitter side))
AH: Asymmetric H-bridge
AX: Single IGBT + series diode on collector side (reverse blocking)
AY: Single IGBT + series diode on emitter side (reverse blocking)
B: Dual module (halfbridge)
BD: Dual module (halfbridge) + 2 diodes in series (reverse blocking)
D: 6-pack (three-phase-bridge)
DL: 7-pack (three-phase-bridge + AL-chopper)
H: Full single phase H-bridge
M: 2 IGBTs in collector connection

Collector-emitter voltage grade (V_{CE}/V/100)

IGBT-series no.
0: first generation 1988-1991 (collector current grade specified at T_{case} = 80°C)
1, 2: first generation 1992-1996 (collector current grade specified at T_{case} = 25°C)
(600V-types: PT-IGBTs, collector current grade specified at T_{case} = 80°C)
3: second generation (high density-NPT-IGBTs for 600 V and 1200 V),
first generation NPT-IGBT-chips for 1700 V, CAL-diodes;
600 V-types: collector current grade specified at T_{case} = 80°C,
1200 V-/1700 V-types: collector current grade specified at T_{case} = 25°C;
low inductance case
4: high density, lowV_{CEsat}-NPT-IGBT-chips (1200 V, 1700 V)
5: high density, high speed-NPT-IGBT-chips (600 V, 1200 V)
6: Trench-NPT-IGBT-Chips

Features
D: fast inverse diode
K: SEMITRANS 5-case with screw connectors
L: 6-pack-case with solder pins
S: Collector-Sense-Terminal
I: enlarged inverse diode (higher power capability)

SKiiP converter in an automobile with hybrid drive ▷

SEMITOP power modules

The SEMIKRON SEMITOP module range comprises solderable power modules with thyristors, diodes, power MOSFETs and IGBTs; in the following only SEMITOPs with MOSFETs and IGBTs are considered,

e.g. **SK 100 G B 12 3 x**

SEMIKRON component

Current rating in A at $T_h = 25°C$

G: IGBT-switch
M: MOSFET-switch

Circuit
A: Single switch
AL: Chopper module (IGBT/MOSFET + free-wheeling diode at collector side)
AR: Chopper module (IGBT/MOSFET + free-wheeling diode at emitter side)
AH: Asymmetric H-bridge
B: Dual module (halfbridge)
D: 6-pack (three-phase-bridge)
H: Full single phase H-bridge

Voltage grade (V_{CE}/V/100 or V_{DS}/V/100)

IGBT-series
2: PT-IGBT-chips (only for 600 V)
3: high density-NPT-IGBT-chips
4: high density, low V_{CEsat}-NPT-IGBT-chips
5: high density, high speed-NPT-IGBT-chips

Features (not yet defined for SEMITOPs with IGBT and MOSFET-chips)

The fast inverse diode(s) integrated in every IGBT-SEMITOP are not indicated in the designation code.

1.5 Examples for new packaging technologies

New packaging technologies are being developed mainly with regard to:
- improvement of heat dissipation and temperature cycling capability,
- minimized inductances in the module and in the supply leads by means of suitable module construction,
- highly flexible assembly and connection technology, easy mounting at the user's facilities,
- higher complexity of integration (converter circuits),
- integration of monitoring, protection and driver functions,
- delivery of tested electric or thermal-electrical systems.

The following four ranges of power modules, which have been developed with consideration to the requirements mentioned above, are therefore regarded as exemplary.

1.5.1 SKiiPPACK

Figure 1.58 shows the scheme of a SKiiPPACK (**S**emi**k**ron **i**ntegrated **i**ntelligent **P**ower **Pack**).

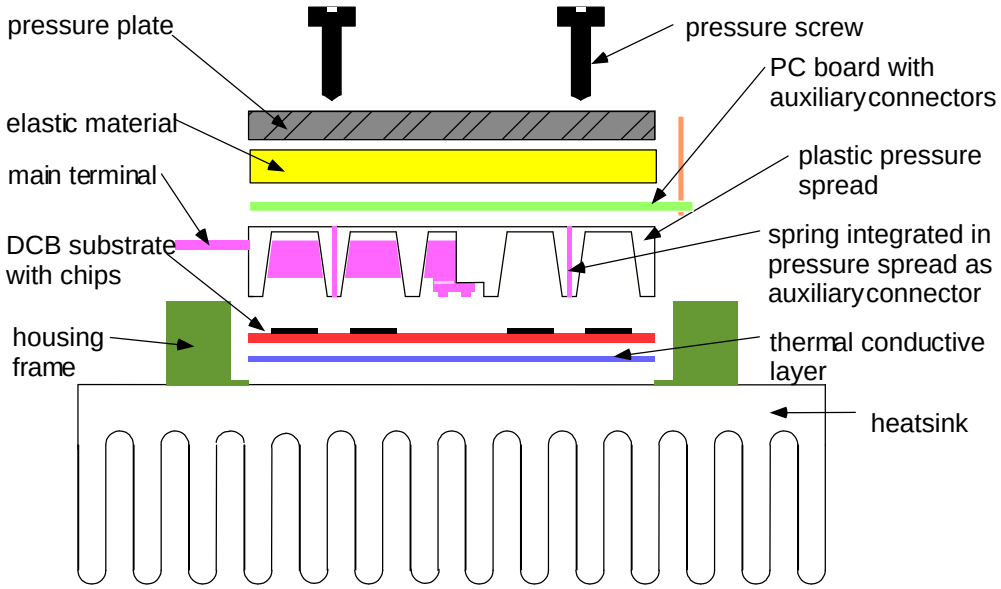


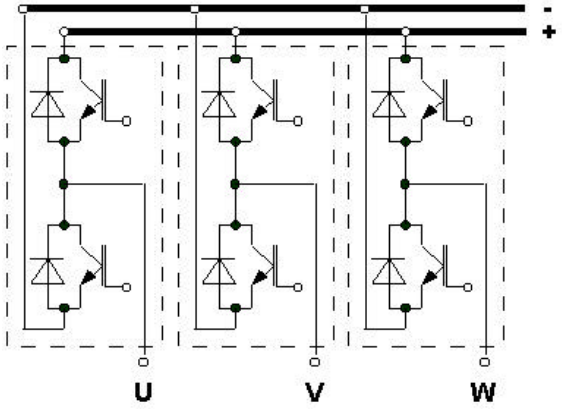
Figure 1.58 Basic SKiiPPACK structure

In contrast to conventional transistor modules, the DCB-substrates carrying the IGBT and diode chips are not soldered on to a copper base plate, but are pressed almost with the complete surface directly to the heatsink by means of a plastic pressure spread. The electrical connection of the DCB to the SKiiPPACK terminals, designed for connection of laminated, low-inductance busbars, is made by pressure contacts and low-inductive track layout. A metal plate serves as pressure element and as thermal and EMI-shield for the driver circuit, which is also integrated into the SKiiP case.
By paralleling many, relatively small IGBT-chips and with their optimal contact to the heatsink, the thermal resistance may be reduced considerably compared to standard modules, since the heat is spread evenly over the heatsink.

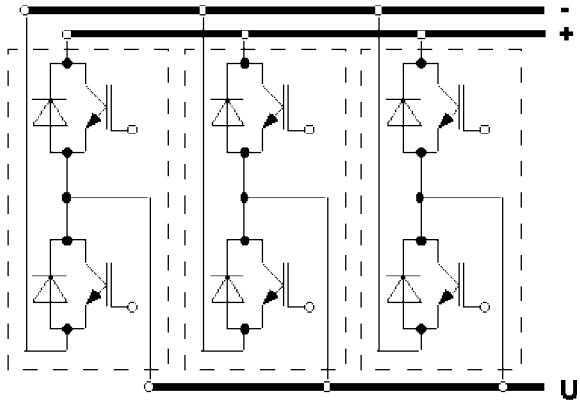
Three sizes of cases (2, 3 and 4 arms in GB, GAL or GAR-configuration) and different chip arrangements as well as adapted driver components connected by simple external constructions guarantee the realization of dual modules, H-bridges, SIXPACKS and SEVENPACKs in 600 V-, 1200 V- and 1700 V-technology. 3300 V-SKiiPPACKs are under development.

In Figure 1.59 the special flexibility of the SKiiPPACK principle is explained with an example.

a)



b)



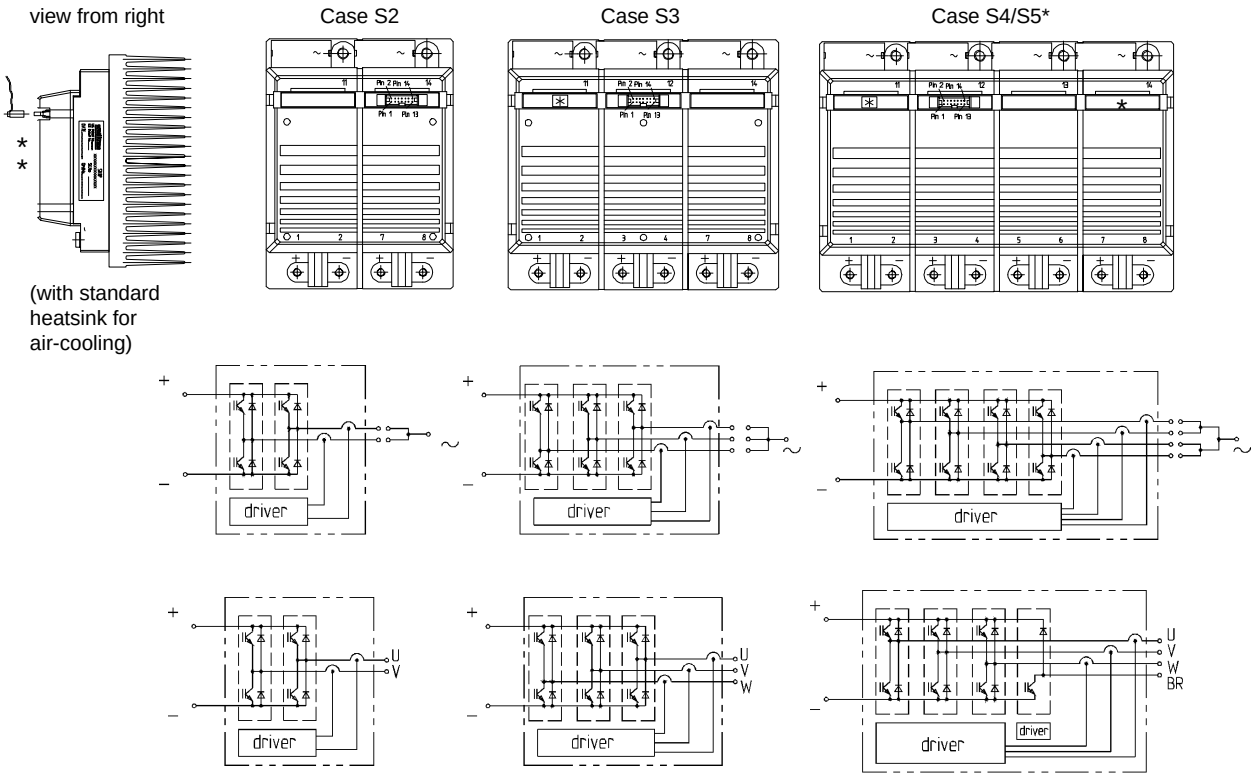
c)

Figure 1.59 Possible applications of a SKiiPPACK with 3 identical DCBs (example)
a) View of a SKiiPPACK on an aluminium heatsink
b) SIXPACK
c) Dual module (halfbridge)

Besides transistor and diode chips, PTC-temperature sensors are integrated into the DCB; their output signal directly affects driver operation (temperature limit) and - due to analogous amplification in the driver - it can also be used for evaluation of the heatsink temperature.
The AC-connectors of the SKiiPPACK accommodate current sensors for overcurrent and short-circuit protection of the IGBTs. Signal processing and linkage is done by the internal driver, which is positioned on the pressure plate; this will be described in detail in chapters 1.6 and 3.5.8. The potential-free current signals may also be used as actual values for external sensors and control circuits.

Advantages offered by SKiiPPACKs in comparison to conventional modules are:
- improved temperature cycling capability,
- reduced thermal resistance by direct heat transfer chip-DCB-heatsink,
- possibility of producing very compact constructions with high power density,
- low switching overvoltages due to thorough low-inductive structure, i.e. high permissible DC-link voltage and reduction of interference generation,
- repairable and recyclable by excluding hard moulding and internal soldering,
- optimal adjustment of internal, intelligent driver,
- load test of complete systems carried out at manufacturer.

Figure 1.60 shows SKiiPPACK cases and some of standard internal circuits. Further circuits are available and may be integrated if required by the customer, respectively (e.g. brake chopper, asymmetrical bridges).
Besides the heatsink shown below, other air or water-cooled heatsinks may also be used for mounting of the SKiiPPACKs.



* case S5 has an additional DIN-Connector on the right quarter of top (for brake-chopper-input)

** F-Option: fibre optic connectors for driver input and fault detector output

Figure 1.60 SKiiPPACK cases and standard internal circuits

1.5.2 MiniSKiiP

Another new development for the low-power range, which is outstanding for its special flexibility and easy mounting is SEMIKRON's MiniSKiiP with pressure contacts, the basic structure of which is shown in Figure 1.61.

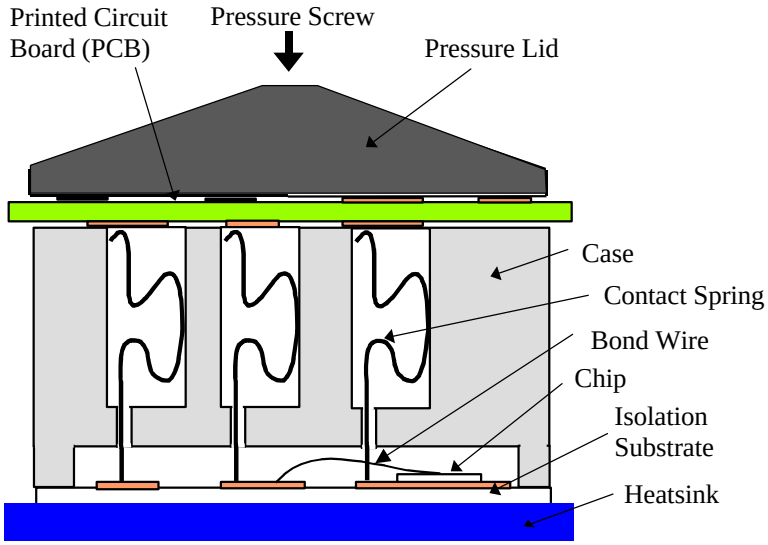


Figure 1.61 Basic structure of a MiniSKiiP

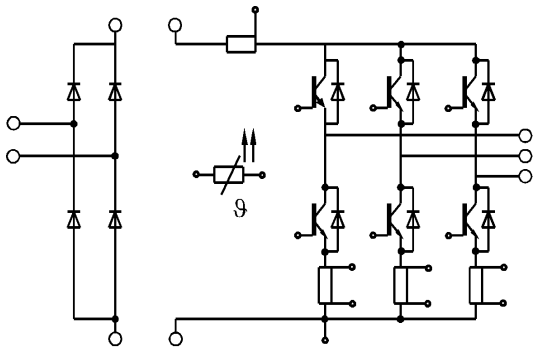
Basic elements of a MiniSKiiP are:
- DCB isolation substrate with soldered, wire-bonded semiconductor chips (e.g. IGBTs, MOSFETs, diodes, thyristors) as well as other components, such as current and temperature sensors, resistors and capacitors,
- silicone filled case with integrated contact springs and glued in DCB and
- hard plastic cover.

One or two screws take care of all electrical and thermal connections (to the heatsink) making a detachable connection between SKiiP cover, PCB, MiniSKiiP and heatsink. The contact springs have several functions: they serve as the electrical connection between the power semiconductors on the DCB and the other circuits on the PCB, and also as pressure spring pad between DCB and heatsink in the mounted state.
The high number of springs spread over the total MiniSKiiP area provides for even pressure between components and heatsink, which guarantees a low thermal resistance.

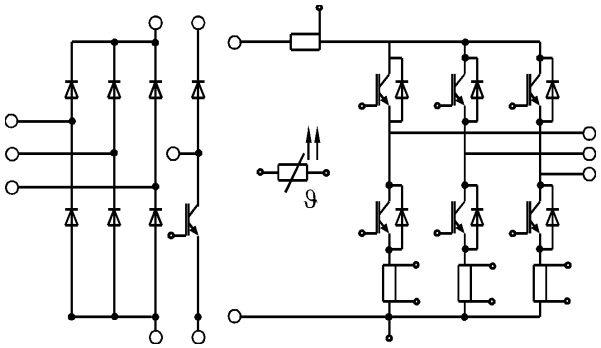
For the current range above 10 A, the contacts are connected in parallel. The multitude of spring shafts results in a high degree of flexibility concerning the production of many different circuits for drives and power supplies as well as other applications.

Several types of cases designed for different power ranges are available from MiniSKiiP 1 (line voltage up to 230 V, rated current up to 12 A) to MiniSKiiP 8 (line voltage up to 400 V, rated current up to 125 A) (Figure 1.62).

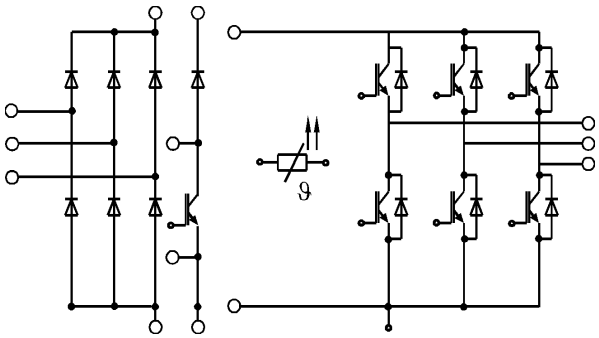
MiniSKiiP
Case M 1



MiniSKiiP
Case M 2

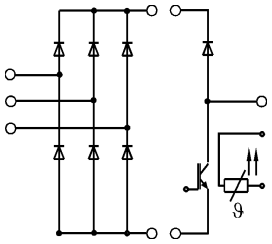


MiniSKiiP
Case M 3



MiniSKiiP
Case M 8a; Case M 8

M 8a



M 8

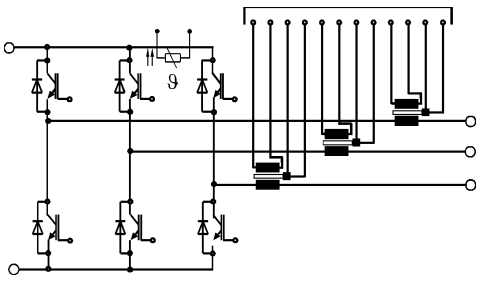


Figure 1.62 Standard MiniSKiiP types and circuits

In the biggest MiniSKiiP (MiniSKiiP 8) curved, pressure contact springs are used because of the high currents applied; these can be supported by compensating current sensors on the AC-side. (Figure 1.63).

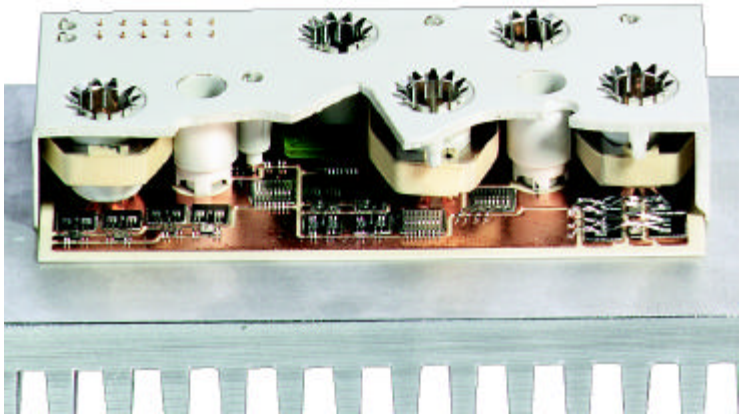


Figure 1.63 MiniSKiiP 8 curved springs with current sensors

In order to avoid too high a concentration of heat sources, the standard circuit is divided up over two cases, one of them containing the uncontrolled or half-controlled bridge rectifier and the brake chopper, the other containing the three-phase-converter.

1.5.3 SEMITOP

The product range of SEMITOP, which has already been mentioned, comprises 3 types of cases (see Figure 1.57).
Just like SKiiPPACK and MiniSKiiP, SEMITOP is also assigned to those constructions without base plate that generate widespread pressure of the DCB to the heatsink by a special construction of the plastic housing.
One or two screws make a closed linkage between module and heatsink. In contrast to MiniSKiiP the contacts to the PCB are made by two lines of solder pins.
Due to the ability of such a small module to integrate up to 12 power components, SEMITOP is used preferably in low-size applications. The unrestricted useability of the space between the solder pins for other printed circuit board components is advantageous in comparison to MiniSKiiP, which is very similar in its technology.

1.5.4 New low-inductive IGBT module constructions for high currents and voltages

A very interesting and promising development in high-power electronics (e.g. 1.2 kA and 2.5/3.3 kV) is the low-inductive FLIP-module (ABB Semiconductors, [6]) and the SKiM20-module (without base plate) by SEMIKRON (Figure 1.64).
These modules had been designed especially for high-power range. Therefore, the development goals had been mainly high reliability (high power and temperature cycling capability), good heat dissipation behaviour (decentralized heat sources / low thermal resistances), minimized inductances in the module and module busbarring as well as safe failure behaviour (explosion protection by means of defined areas for pressure balancing).
Figure 1.64 shows the basic assembly of a SKiM20-module as the most modern version of such module constructions.

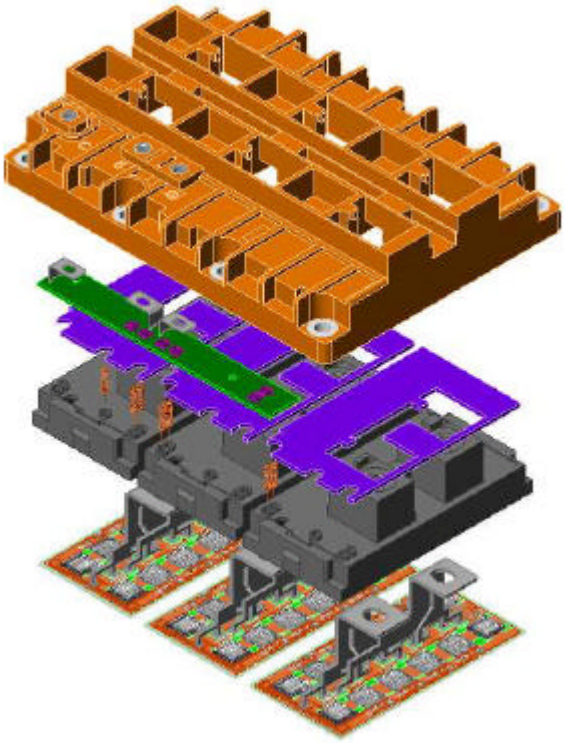


Figure 1.64 Construction of an IGBT-module SKiM20

As the other SKiM-models shown in Figure 1.57 the SKiM20 has no base plate. From this the advantageous basic features discussed in chapter 1.4.2.4 (Figure 1.54) result. The semiconductor chips are arranged on three small areas of AlN ceramic substrates.
One ceramic substrate combined with a case element and a pressure spread element made from plastic as well as a pressure plate forms a sub-module. The pressure spread element presses the substrate almost over its full area to the heatsink. The main terminals of each sub-module are soldered to the substrate. The control and auxiliary terminals are made as pressure contacts.
The case cover also acts as pressure element.

1.6 Integration of sensors, protective functions, drivers and intelligence

In the following, some examples for the integration of peripheral functions in power modules are described, sorted by increasing degrees of integration.

Sense IGBT-Module

Sense IGBT-modules contain sense-IGBTs as described in chapter 1.2.4.

Compared to solutions with shunts in the emitter circuit, a much higher measuring resistance may be chosen. Other than with overcurrent protection by V_{CE}-monitoring, either shorter dead-times are required or none at all.

Modules with integrated temperature sensor

As an alternative to the *TEMPFET* (see chapter 1.2.4) as a solution for discrete power semiconductors, simple PTC-temperature sensors in SMD-design are being used in modules more and more, with a higher degree of integration; they are soldered on to the DCB-substrate near the chips.
The heatsink temperature is indicated at a defined point by the sensors. Ideally, the transversal heat flow between this point and the heatsink areas under the hottest chips may be neglected. A suitable evaluation board takes care of overtemperature protection by active control on the driver or processing the analogous signal.

Rugged Modules [281]

Besides the IGBT hybrid protective circuit are integrated into the case for protection of the IGBT in case of failure. The terminal behaviour are determined by the driver just as with conventional IGBTs; the protective circuits are activated only in case of failure and will limit the short-circuit current.

*IPM (**I**ntelligent **P**ower **M**odules) [280]*

IPM modules are able to integrate, in addition to the IGBTs and free-wheeling diodes, drivers and protective units (IPM minimal configuration) as well as complete inverter control units. The user, himself, can no longer control switching and on-state characteristics, therefore IPMs are often designed specifically for the application (ASIPM = **A**ppl. **S**pecif. **IPM**).

*SKiiPPACKs (**S**emi**k**ron **i**ntegrated **i**ntelligent **P**ower **Packs**)*

As already described in chapter 1.5.1, SKiiPPACKs contain a driver unit, laid out as an SMD-PCB, which integrates all the necessary protective and monitoring functions and which is positioned over the pressure plate. (see Figure 1.58).

SKiiPPACKs may be driven and supplied on potential of the superordinated control system (CMOS or TTL level). The SKiiPPACK driver integrates all necessary potential separation, a SMPS and the power drivers.

SKiiPPACKs are equipped with current sensors in the AC-outputs and temperature sensors as well as an optional DC-link voltage sensor. The driver valuates the signals transmitted by the sensors in order to care for overcurrent/ short-circuit, overtemperature and overvoltage protection as well as supply-undervoltage protection. An error signal and standardized analogous voltage signals of the actual AC-output current value, the actual heatsink temperature and, optionally, the DC-link voltage are available on separate potentials at the driver connector for evaluation in the superordinate control circuit.

Figure 1.65 describes the OCP (**O**ver **C**urrent **P**rotection) driver principle, which will be detailed in chapter 3.5.8.

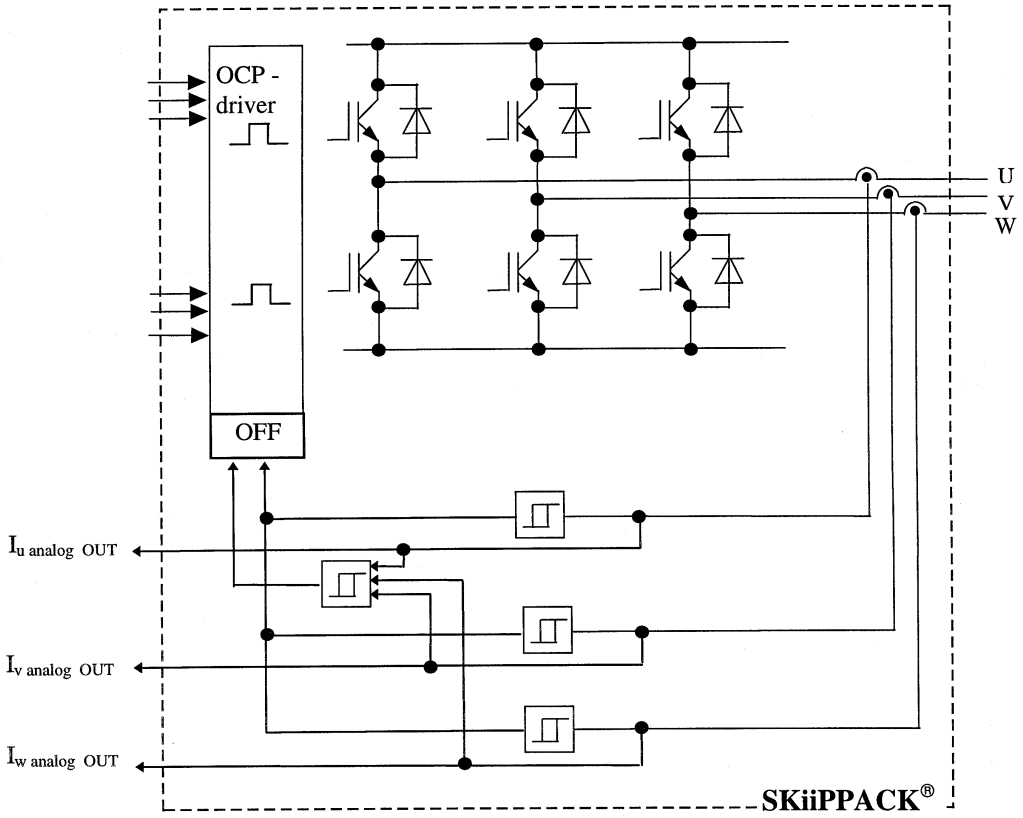


Figure 1.65 OCP-driver principle [264], [265]

2 Datasheet parameters for MOSFET, IGBT, MiniSKiiP- and SKiiPPACK modules

2.1 General

2.1.1 Letter symbols, terms, standards

Letter symbols and terms [264], [265]

Voltages: firstly, two index letters are used to indicate the terminals between which the applied voltage is taken. If the potential of the terminal designated with the first index letter is positive versus the terminal designated with the second index letter (reference potential), the applied voltage is positive, e.g. V_{CE}.

As for diodes, "F" is used for the forward on-state voltage (positive anode potential versus cathode potential) and "R" for the reverse blocking voltage (positive cathode potential versus anode potential).
As for transistors, an additional third index letter may indicate the type of circuit between terminal 2 and a non-designated third terminal, e.g. V_{CGR}, where the third letter symbol is defined as follows:
S: short-circuit between terminal 2 and 3,
R: resistor to be specified between terminal 2 and 3,
V: external voltage between terminal 2 and 3, to be specified,
X: resistor and external voltage between terminal 2 and 3, to be specified.

Index letters can be followed or preceded by other index abbreviations for further specification of parameters, either with or without brackets and either as capital or small letters (e.g. $V_{(BR)DS}$ or $V_{GE(th)}$ or V_{CEsat}), for example:
(BR): breakdown voltage,
sat: saturation voltage,
(th): threshold voltage,
clamp: clamping voltage limited by external circuits.

Supply voltages are often marked by doubleindex letters, e.g. V_{GG} (supply voltage of gate-emitter circuit), V_{CC}, V_{DD}.

Currents: at least one index letter is used to specify a current. Positive values specify positive currents, which enter the component at the terminal and are named first in the index, e.g. I_{GE}. If there is no danger of mix-up, only the first index letter is usually used, e.g. I_C (collector current), I_D, I_G. The same applies when indicating negative currents.

As for diodes, "F" is used for indicating forward on-state currents (anode-cathode) and "R" for reverse currents (cathode-anode).
As for transistors, an additional third index letter may indicate the type of circuit between terminal 2 and a non-designated third terminal, e.g. I_{GES}, where the third letter symbol is defined as follows:
S: short-circuit between terminal 2 and 3,
R: resistor to be specified between terminal 2 and 3,
V: external voltage between terminal 2 and 3, to be specified,
X: resistor and external voltage between terminal 2 and 3, to be specified.

Index letters can be followed or preceded by other index abbreviations, either with or without brackets and either as capital or small letters, for example:
AV : average value,
RMS: effective value, (root mean square)
M: peak value (maximum),
R: periodic (repetitive),
S: non-periodic (spike),
puls: pulsed (direct current).

Other symbols: the terminology used for other symbol indications for electrical, thermal and mechanical parameters mainly follows the terminology for voltages and currents; for further explanation please see the following table. Index letters may also specify turn-on (on) and turn-off (off) switching states (mostly in brackets).

Standards for terms and definitions

Details with regard to definitions, determination of terms, datasheet parameters and measurement procedures may be taken, for example, from the following standards:

Standards, terms and definitions

DIN 40 900 T5	Semiconductors, switching symbols
DIN 41 781	Diodes: terms and definitions
DIN 41 785 T3	Power semiconductors: symbols
DIN 41 858	Field effect transistors: terms and definitions
IEC 191-1...4	Mechanical standards (cases)
IEC 50 (521) 1984, (551) 1982	International dictionary for electrical engineering
IEC 617-5	Graphic symbols, switching symbols for diagrams
IEC 971 (1989-07)	Semiconductor converters: designation system

Datasheet parameters and measurement procedures

DIN 41 791 T1	Principle designations for datasheets
DIN 41 792 T2	Test procedures: diodes
T3	Test procedures: heat resistance
IEC 747-1: 1983	Semiconductor components/ Volume 1: General hints with reference to maximum ratings and characteristics, test procedures
IEC 747-2: 1983, A1(1992), A2(1993)	Rectifier diodes
IEC 747-8: 1984, A1(1991), A2(1993)	Field effect transistors
IEC 60747-9: 1998 FDIS	IGBTs (in preparation)

R & D standards and reliability

IEC 664-1: 1992	Co-ordination for the isolation of electrical appliances < 1 kVeff Volume 1: principles, test procedures
IEC 146-1-1: 1991/EN60146-1-1: 1993	Semiconductor converters: basic requirements
DIN EN50178 (VDE0160): 4/1998	Electronic devices for power systems: general isolation test procedures
IEC 947-4-2/EN60947-4-2:1997	Designation system for low-voltage appliances, volume 4.
UL 1557: 5/1993	Inflammability, isolation safety

UL 94-V0: 9/1981	Inflammability of plastic materials
IEC 747-1, IX: 1983	Components at risk of ESD (**E**lectro**s**tatic **D**ischarge)
DIN IEC 68-2-...	Reliability tests
ISO 9001/EN29001: 1995	Quality system certification
DIN EN ISO 9001: 8/1994	Re-qualification of quality system

2.1.2 Maximum ratings and characteristics

Maximum ratings

Maximum ratings for modules indicated in the datasheets are extreme values of electrical, thermal and mechanical load permissible without risk of destruction or damage. Every limit value has been specified according to exactly defined conditions, which have inevitably to be indicated in the datasheets, since some of these conditions have not (yet) been standardized.
Exceeding one of the maximum ratings may lead to destruction of the component, even if other maximum ratings have not been strained to their utmost limit.
In addition to the “static“ maximum ratings listed in the following there are so-called “dynamic“ maximum ratings, which designate the permissible course of the characteristics (current/ voltage) during switching.
If not otherwise shown, the maximum ratings in the datasheets are valid at a chip or case temperature of 25°C, for higher temperatures deratings usually have to be considered.

Characteristics

Characteristics describe the features of components determined under certain specified measuring conditions (mostly application-specific).
Just as with maximum ratings, all characteristics are subject to exactly specified ambient conditions which have to be indicated in the datasheets, since some of those conditions are also not standardized.
Characteristics are often indicated as typical values within a range.
The reference temperatures for chip or case are normally indicated with e.g. 25°C or 125°C so temperature dependency has to be considered in the case of differing temperatures.
Limits and characteristics are published in the form of tables and diagrams.

2.2 Power MOSFET modules [264], [265]

2.2.1 Maximum ratings

MOSFETs/module structure

Drain-source voltage V_{DS}
Maximum voltage between drain and source contacts of MOSFET chips for open or closed gate-source circuit.
Parameter: case temperature T_{case} = 25°C

Drain-gate voltage V_{DGR}
Maximum voltage between drain and gate,
Parameters: external resistance R_{GS} between gate and source, case temperature T_{case} = 25°C

Continuous direct drain current I_D
Maximum direct current at drain output
Parameters: case temperature, e.g. T_{case} = 25°C, 80°C: I_D@25°C, I_D@80°C

Peak value of a periodic drain current I_{DM} or pulsed drain current I_{Dpuls}
Peak value of current at drain output during pulse operation,
Parameters: pulse duration t_p, case temperature, e.g. T_{case} = 25°C, 80°C and pulse/break ratio (diagram "maximum safe operating area")

Single pulse avalanche energy dissipation E_{AS}
Maximum avalanche energy dissipation from drain to source of a single chip during turn-off of an unclamped inductive load (single pulse load),
Parameters: instantaneous drain current i_D, drain-source supply voltage V_{DD}, external gate-source resistance R_{GS}, external drain inductance L, chip temperature, e.g. T_j = 25°C

Gate-source voltage V_{GSS} or V_{GS}
Maximum voltage between gate and source
Parameter: case temperature T_{case} = 25°C

Total power dissipation P_{tot} or P_D
Maximum power dissipation per transistor/diode or within the whole power module $P_{tot} = (T_{jmax}-T_{case})/R_{thjc}$,
Parameter: case temperature T_{case} = 25°C

Operating temperature range T_{vj} or T_j ; $T_{j(min)}$....$T_{j(max)}$
Permissible chip temperature range within which the module may be permanently operated

Storage temperature range T_{stg}; $T_{stg(min)}$....$T_{stg(max)}$)
Temperature range within which the module may be stored or transported without being subject to electrical load.

Isolation test voltage V_{isol} or V_{is}
Effective value of the permissible test voltage between input terminals/ control terminals (short-circuited, all terminals connected to each other) and module base plate.
Parameters: test duration (1 min, 1 s), rate of rise of test voltage, if required;
according to IEC 146-1-1 (1991), EN 60146-1-1 (1993), section 4.2.1 (corresponds to VDE 0558, volume 1-1: 1993-04) and DIN VDE 0160 (1988-05), section 7.6 (corresponds to EN 50178 (1994)/ E VDE 0160 (1994-11) the test voltage shall only rise gradually up to its maximum rating.

Grade of humidity
describes the permissible ambient conditions (atmospheric humidity) according to DIN 40 040

Grade of climate
describes the permissible ambient test conditions (climate) according to DIN IEC 68-1

Inverse diodes/ free-wheeling diodes

Forward current I_F
Maximum forward current value of inverse or free-wheeling diodes,
Parameter: case temperature, e.g. T_{case} = 25°C, 80°C

Peak forward current I_{FM} or pulsed forward current I_{Fpuls}
Peak value of diode current during pulse operation
Parameters: pulse duration t_p, case temperature, e.g. T_{case} = 25°C, 80°C

2.2.2 Characteristics

MOSFETs/ module structure

Drain-source breakdown voltage$V_{(BR)DSS}$
Breakdown voltage between drain and source, gate-source short-circuited (V_{GS} = 0)
Parameters: Reverse drain current I_D, case temperature T_{case} = 25°C

Gate-source threshold voltage $V_{GS(th)}$
Gate-source voltage above which considerable drain current will flow,
Parameters: drain-source voltage $V_{DS} = V_{GS}$, drain current I_D, case temperature T_{case} = 25°C

Zero gate voltage drain current I_{DSS}
Blocking current between drain and source with gate-source short-circuited (V_{GS} = 0) and drain-source voltage $V_{DS} = V_{DSS}$,
Parameter: chip temperature, e.g. T_j = 25°C and 125°C

Gate-source leakage current I_{GSS}
Leakage current between gate and source with drain-source short-circuited (V_{DS} = 0) at maximum gate-source voltage V_{GS},
Parameters: gate-source voltage V_{GS}, case temperature T_{case} = 25°C

Drain-source on-resistance $R_{DS(on)}$
Quotient of changing drain-source voltageV_{DS} and drain current I_D in a thoroughly gate-controlled MOSFET at a specified gate-source voltage V_{GS} and a specified drain current I_D (at "rated current"),
In this state V_{DS} is proportional to I_D, during large-signal behaviour the forward on-state voltage $V_{DS(on)} = R_{DS(on)} * I_D$.
Parameters: gate-source voltage V_{GS}, drain current I_D ("rated current"), case temperature T_{case} = 25°C ($R_{DS(on)}$ is extremely dependent on temperature!).

Forward transconductance g_{fs}
Quotient of changing drain current and gate-source voltage at a specified drain current I_D (at "rated current"),
Parameters: drain-source voltage V_{DS}, drain current I_D ("rated current"), case temperature T_{case} = 25°C

Capacitance chip-case C_{CHC}
Capacitance between a sub-component and the case base plate or the heatsink potential,
Parameter: case temperature T_{case} = 25°C

Input capacitance C_{iss}
Capacitance between gate and source with drain-source short-circuited for AC and gate-source voltage $V_{GS} = 0$.
Parameters: drain-source voltage V_{DS}, measuring frequency f, case temperature $T_{case} = 25°C$

Output capacitance C_{oss}
Capacitance between drain and source with gate-source short-circuited ($V_{GS} = 0$),
Parameters: drain-source voltage V_{DS}, measuring frequency f, case temperature $T_{case} = 25°C$

Reverse transfer capacitance (Miller capacitance) C_{rss}, C_{mi}
Capacitance between drain and gate with drain-source short-circuited at AC and gate-source voltage $V_{GS} = 0$. For measuring, the source has to be connected with the protective shield of the measuring bridge.
Parameters: drain-source voltage V_{DS}, measuring frequency f, case temperature $T_{case} = 25°C$

Parasitic drain-source inductance L_{DS}
Inductance between drain and source

Switching times
Switching times indicated in MOSFET datasheets are determined from a measuring circuit under ohmic load according to Figure 2.1a. They refer to the gate-source characteristics during turn-on and turn-off, see Figure 2.1b.
Switching times as well as real current and voltage characteristics are determined by internal capacitances, inductances and resistances and by those of the gate and drain circuit; for this reason, all indications in the datasheets and the characteristics depicted therein may serve only as a guide.

As the current and voltage characteristics are not relevant to most applications, because they are based on the application of pure ohmic load, their importance is actually restricted to the definition of switching times.
The waveforms will deviate significantly especially if inductive or capacitive loads are involved (chapter 1.2.3) and also the measurement results may differ.

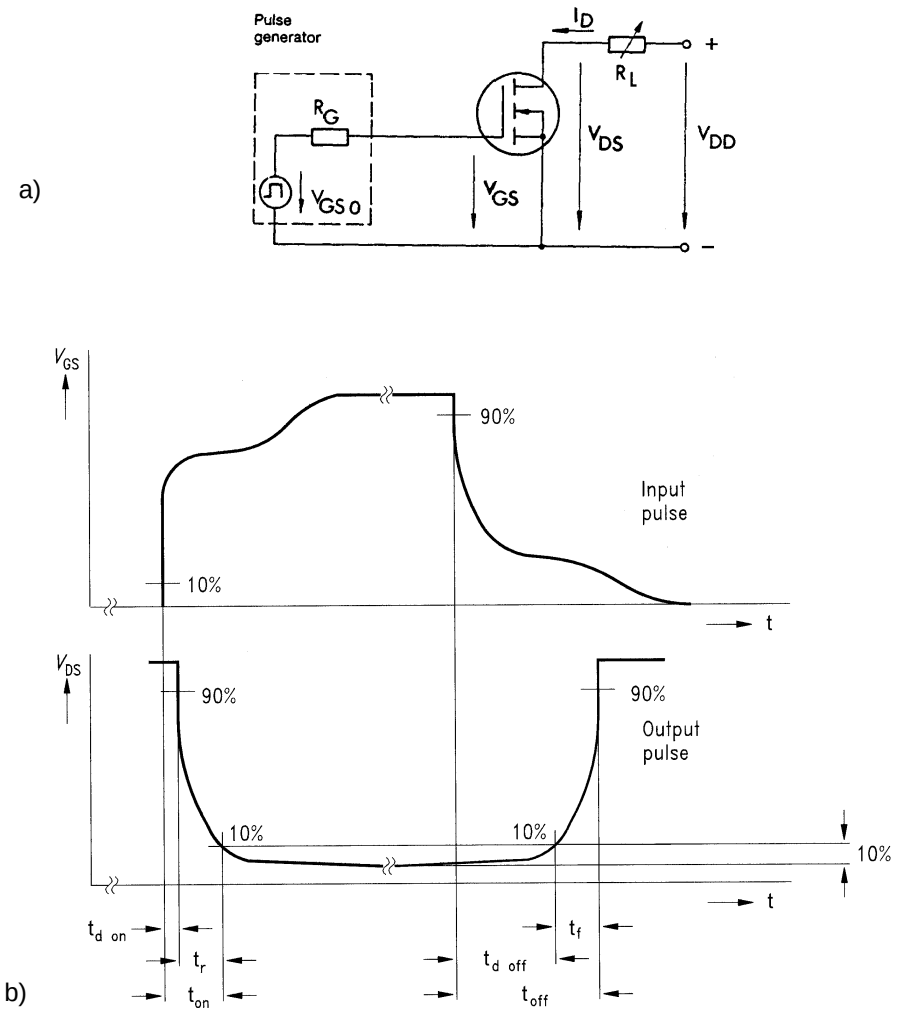


Figure 2.1 a) Measuring circuit
b) Definition of MOSFET switching times under ohmic load

The following parameters are indicated relevant to switching times:
measuring circuit, drain-source supply voltage V_{DD}, gate-source control voltage V_{GS}, drain current I_D, gate series resistance R_G (internal resistance of the control circuit), sometimes gate-source resistance R_{GS}, case temperature T_{case} = 25°C.

Turn-on delay time $t_{d(on)}$
After sudden turn-on of a positive gate-source control voltage V_{GG}, the gate-source voltage V_{GS} starts to rise with a time constant determined by input capacitance and gate resistance. As soon as the threshold voltage $V_{GS(th)}$ has been reached, the drain-source voltage V_{DS} will start to decrease and the drain current I_D will begin to rise.
The **turn-on delay time $t_{d(on)}$** is defined as the time interval between the moment when the gate-emitter voltage V_{GE} has reached 10 % of its end value (V_{GG}), and when the drain-source voltage has dropped to 90 % of its initial value (V_{DD}) .

Rise time t_r
The **rise time t_r** is defined as the time interval following the turn-on delay time, where the drain-source voltage drops from 90 % to 10 % of its initial value (V_{DD}). During this time, the drain

current will rise (therefore “rise time”), i.e. the major part of the turn-on losses is generated during this time interval.

The sum of **turn-on delay time $t_{d(on)}$** and **rise time t_r** is called **turn-on time t_{on}**.
As the drain-source voltage V_{DS} will not yet have reached its forward on-state value $V_{DS(on)} = R_{DS(on)} * I_D$ at the (defined) end of t_{on}, but still amounts to 10 % of V_{DD}, there will still be higher losses after t_{on} than the forward on-state losses.

Turn-off delay time $t_{d(off)}$
After sudden turn-off of the positive gate-source control voltage V_{GG}, the gate-source voltage V_{GS} starts to decline with a time constant determined by the input capacitance of the MOSFET and the gate-source resistance R_{GS}. The drain current which is coupled with the gate voltage in the active operating area via forward transconductance $g_{fs} = di_D/dv_{GS}$ also begins to decrease, whereas the drain-source voltage starts to rise accordingly.
The **turn-off delay time $t_{d(off)}$** is defined as the time interval between the moment when the gate-emitter voltage V_{GE} has declined to 90 % of its initial value (V_{GG}), and the drain-source voltage has risen to 10 % of the supply voltage V_{DD}.

Fall time t_f
The **fall time t_f** is defined as the time interval following the turn-off delay time, where the drain-source voltage rises from 10 % to 90 % of its end value V_{DD}. During this time, the drain current will fall accordingly (therefore “fall time”), i.e. most of the turn-off losses are generated here.

The sum of **turn-off delay time $t_{d(off)}$** and **fall time t_f** is called **turn-off time t_{off}**.
As the drain current I_D will not have dropped to cut-off current level at the defined end of t_{off}, but still amounts to 10 % of its forward on-state value, there will still be higher losses after t_{off} than the blocking losses.

Internal thermal resistance junction to case R_{thjc} per MOSFET
The thermal resistance R_{thjc} describes the passage of heat between the MOSFET chips (index j) and the module case (index c). It characterizes the static heat dissipation of a MOSFET system within a module (mostly consisting of paralleled chips) and depends on chip size and module assembly.
The temperature difference ΔT_{jc} between chip temperature T_j and case temperature T_{case} at a constant power dissipation P is defined as follows: $\Delta T_{jc} = T_j - T_{case} = P * R_{thjc}$.

Contact thermal resistance case to heatsink R_{thch} per MOSFET module
The thermal resistance R_{thch} describes the passage of heat between the module case (index c) and the heatsink (index h). It characterizes the static heat dissipation of a MOSFET module (possibly with several MOSFET switches) and depends on module size, heatsink and case surfaces, thickness and parameters of thermal layers (pastes, foils, print covers) between module and heatsink as well as on the mounting torque of the fixing screws.
The temperature difference ΔT_{ch} between case temperature T_c and heatsink temperature T_h at a constant total amount of single power dissipations P_n within the module is defined as follows: $\Delta T_{ch} = T_{case} - T_h = P_n * R_{thch}$.

Separate determination of R_{thjc} and R_{thch} is not possible for modules without base plate (e.g. SEMITOP, SKiiPPACK, MiniSKiiP). For these module, R_{thjh} is indicated per MOSFET and per module. The temperature differences may be calculated in analogy.

Mechanical data

Apart from the **case construction type,** the following mechanical data are usually indicated in the datasheets:

Mounting torque M_1 of the fixing screws (minimum and maximum value) in Nm or lb.in.;
Mounting torque M_2 of the output terminals (minimum and maximum value) in Nm or lb. in.;
Weight w of the module in g;
Permissible **acceleration under vibration a** in $m*s^{-2}$.

Free-wheeling diodes/ inverse diodes

Inverse diode forward voltage (negative source-drain voltage) V_{SD}, V_F

Negative source-drain voltage drop with gate-source short-circuited (V_{GS} = 0). V_{SD} describes the forward characteristics of the parasitic inverse diodes of the MOSFETs or the hybrid free-wheeling diodes, which are antiparallel to the MOSFETs.
Parameters: forward current I_F; case temperature T_{case} = 25°C

Threshold voltage of the inverse diode $V_{(T0)}$
Forward slope resistance of the inverse diode r_T

With the help of threshold voltage and forward slope resistance a simplified approximation of the forward characteristic may be produced. The threshold voltage indicates the point of crossover with the voltage axis, the forward slope resistance determines the rate of rise of the characteristic.

Reverse recovery time of the inverse diode t_{rr}

Reverse recovery time of the internal or hybrid MOSFET inverse diode during free-wheeling operation, i.e. when a high drain current $-I_D = I_F$ is commutated with a high di_F/dt and a high reverse voltage $V_R = V_{DD}$.
Note: t_{rr} depends very strongly on the temperature (almost doubled value between 25°C and

Parameters: forward current I_F; reverse voltage V_R, rate of fall of forward current $-di_F/dt$, chip temperature T_j = 25°C und 150°C.

Recovered charge of inverse diode Q_{rr}

Recovered charge of internal or hybrid MOSFET inverse diode during free-wheeling operation, i.e. when a high drain current $-I_D = I_F$ is commutated with a high di_F/dt and a high reverse voltage $V_R = V_{DD}$.
Note: Q_{rr} depends very strongly on the temperature (initial value may be doubled or even increased eight-fold between 25°C and 150°C).
Parameters: forward current I_F; reverse voltage V_R, rate of fall of forward current $-di_F/dt$, chip temperature T_j = 25°C and 150°C.

2.2.3 Diagrams

Following the sequence of the datasheets, this chapter will give some hints concerning MOSFET datasheet diagrams. In the case where the diagram concerned is detailed in other chapters, this will be referred to.

Rated power dissipation P_D of a MOSFET module versus case temperature T_{case}

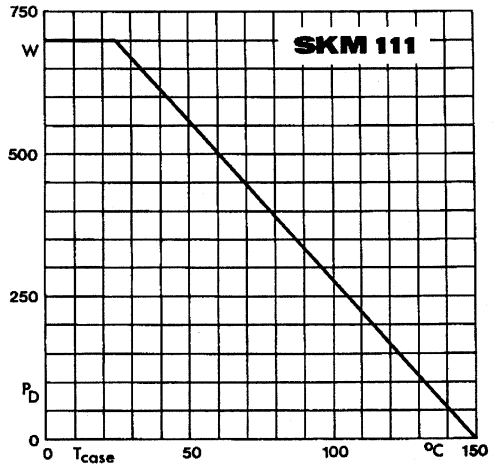


Figure 2.2 Rated power dissipation

Based on the rated power dissipation per MOSFET $P_{D(25°C)} = (T_{jmax} - 25°C)/R_{thjc}$ which is limited to $T_{case} = 25°C$ per definition, the function depicted in the diagram describes derating at a higher case temperature.

Maximum safe operating area during pulse operation (SOA)

As explained in chapter 1.2.3 the MOSFET has to manage an almost rectangular characteristic i = f(u) between V_{DD} and I_L in the case of hard switching.
The SOA (**S**afe **O**perating **A**rea)-diagrams indicate to what extent this may be realized during different operations without risk of destruction:
The SOA is terminated by the following parameters:

- maximum drain current (horizontal termination);
- maximum drain-source voltage (vertical termination);
- maximum power dissipation or chip temperature (diagonal broken termination line in Figure 2.3);
- turn-on resistance (diagonal continuous termination line).

Figure 2.3 shows the maximum curve $I_D = f(V_D)$ during switching and on-state for different pulse durations t_p at a double logarithmic scale.
It is important that the maximum ratings are valid at a case temperature $T_c = 25°C$ and for single pulses, which will not heat the MOSFET over the maximum chip temperature $T_j = 150°$.
Although the lowest of the depicted diagonals represents the hyperbola of the maximum stationary power losses P_{tot}, MOSFET modules may only touch the linear characteristic area during switching operation. Analogous operation over a longer period of time is not permitted, since asymmetries due to spreading among the chips as well as negative temperature coefficients of the threshold voltages might cause thermal instability.

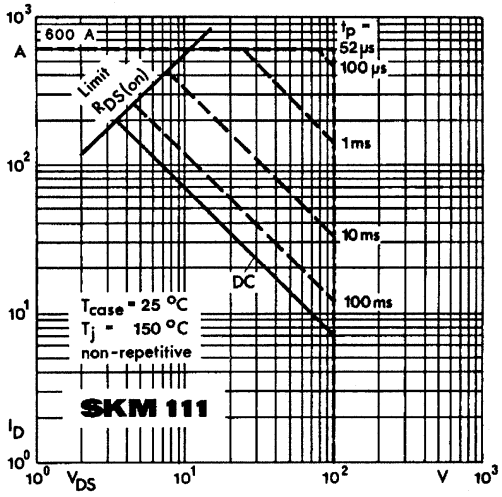


Figure 2.3 Maximum safe operating area $I_D = f(V_{DS})$ during pulse operation (SOA)

Forward output characteristic $I_D = f(V_{DS})$

Figure 2.4 shows the output characteristic (typical values) with parameter V_{GS} (also see chapter 1.2.2.1).

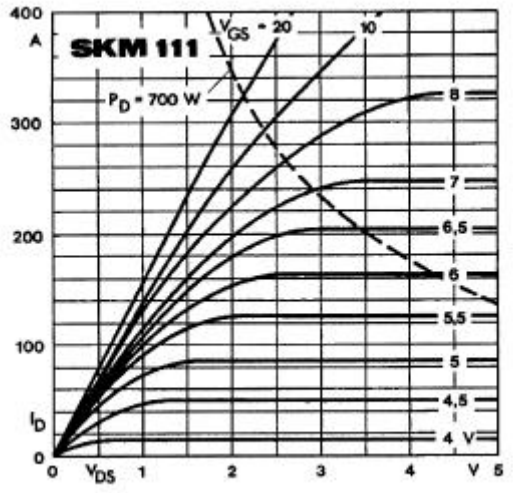


Figure 2.4 Typical MOSFET output characteristic $I_D = f(V_{DS})$ with parameter V_{GS}

Transfer characteristic $I_D = f(V_{GS})$

The transfer characteristic (Figure 2.5) describes the behaviour of the MOSFET in the active operating area at V_{DS} = 25 V (linear operation). The drain current is coupled with the gate-source voltage via $I_D = g_{fs} * (V_{GS}-V_{GS(th)})$.

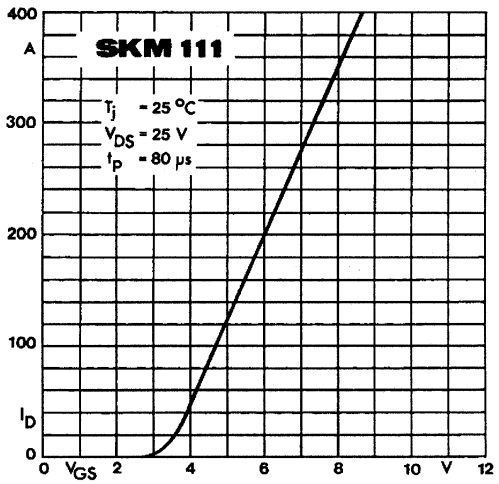


Figure 2.5 Typical transfer characteristic $I_D = f(V_{GS})$

On-resistance versus chip temperature

see chapter 2.6

Drain current derating versus case temperature

see chapter 2.6

Drain-source breakdown voltage versus temperature

As shown in Figure 2.6 the drain-source breakdown voltage of a MOSFET increases linearly to the temperature. As the maximum rating indicated in the datasheets refers to T_j = 25°C, deratings at low chip temperatures have to be accepted .

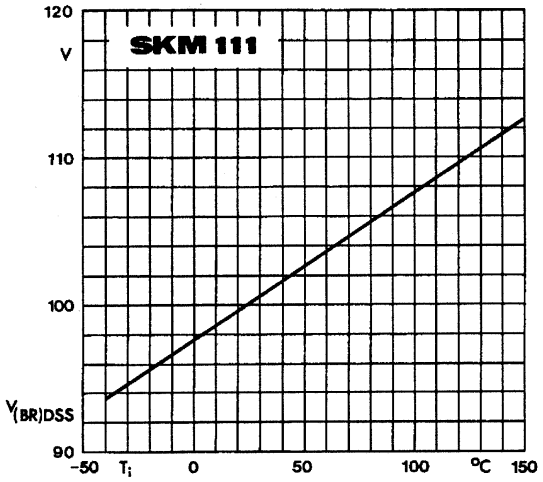


Figure 2.6 Drain-source breakdown voltage $V_{(BR)DSS}$ versus T_j

Drain-source voltage derating versus rate of fall of drain current

see chapter 3.1.1

Internal capacitances versus collector-emitter voltage

see chapter 1.2.3

Gate charge characteristic

see chapter 1.2.3

Diode forward characteristic

see chapter 1.2.2.1

On-resistance versus drain current

Figure 2.7 explains the relationship between on-resistance $R_{DS(on)}$ and drain current I_D or gate-source voltage V_{GS} for a fully controlled MOSFET.

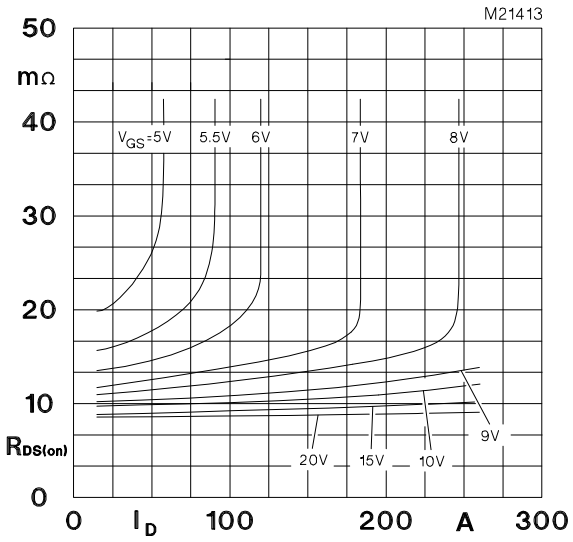


Figure 2.7 Typical characteristic of on-resistance $R_{DS(on)}$ versus drain current I_D and gate-source voltage V_{GS}

The on-resistance decreases with increase of the gate-source voltage. At any point of the curve, a slight increase of $R_{DS(on)}$ together with the drain current has to be considered.

Gate-source threshold voltage versus temperature

Figure 2.8 shows three curves with typical and limit values characterizing the relationship between gate-source threshold voltage $V_{GS(th)}$ and MOSFET chip temperature T_j.

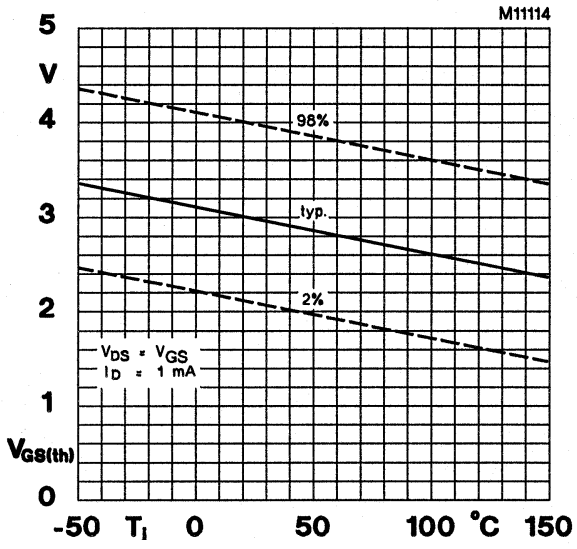


Figure 2.8 Gate-source threshold voltage $V_{GS(th)}$ versus temperature

$V_{GS(th)}$ will decrease linearly when T_j increases. The temperature coefficient of the threshold voltage amounts to about –10 mV/K within the temperature range of -50...+150°C.

Transient thermal impedances for IGBTs and free-wheeling diodes

see chapter 3.2

2.3 IGBT-modules [264], [265]

2.3.1 Maximum ratings

IGBTs/ module structure

Collector-emitter voltage V_{CES} or V_{CE}
Maximum collector-emitter voltage with gate-emitter short-circuited (V_{GE} = 0)
Parameter: case temperature T_{case} = 25°C

Collector-gate voltage V_{CGR}
Maximum collector-gate voltage,
Parameters: external gate-emitter resistance R_{GE}; case temperature T_{case} = 25°C

Continuous collector current I_C
Maximum direct current at collector output
Parameter: case temperature, e.g. T_{case} = 25°C, 80°C: I_C@25°C, I_C@80°C

Peak value of a periodic collector current I_{CM} or pulsed collector current I_{Cpuls}
Peak value of current at collector output during pulse operation
Parameters: pulse duration t_p, case temperature, z.B. T_{case} = 25°C, 80°C and pulse/ break ratio

Gate-emitter voltage V_{GES} or V_{GE}
Maximum gate-emitter voltage
Parameter: case temperature T_{case} = 25°C

Total power dissipation P_{tot}
Maximum power dissipation per transistor/ diode or within the whole power module $P_{tot} = (T_{jmax}-T_{case})/R_{thjc}$,
Parameter: case temperature T_{case} = 25°C

Operating temperature range T_{vj} or T_j ; $T_{j(min)}$....$T_{j(max)}$
Permissible chip temperature range within which the module may be permanently operated.

Storage temperature range T_{stg}; $T_{stg(min)}$....$T_{stg(max)}$)
Temperature range within which the module may be stored or transported without being subject to electrical load.

Isolation test voltage V_{isol} or V_{is}
Effective value of the permissible test voltage between input terminals/ control terminals (short-circuited, all terminals connected to each other) and module base plate.
Parameters: test duration (1 min, 1 s), rate of rise of test voltage, if required;
according to IEC 146-1-1 (1991), EN 60146-1-1 (1993), section 4.2.1 (corresponds to VDE 0558, volume 1-1: 1993-04) and DIN VDE 0160 (1988-05), section 7.6 (corresponds to EN 50178 (1994)/ E VDE 0160 (1994-11) the test voltage shall only rise gradually up to its maximum rating.

Grade of humidity
describes the permissible ambient conditions (atmospheric humidity) according to DIN 40 040

Grade of climate
describes the permissible ambient test conditions (climate) according to DIN IEC 68-1

Inverse diodes/ free-wheeling diodes

Forward current I_F
Maximum forward current value of the inverse or free-wheeling diodes,
Parameter: case temperature, e.g. T_{case} = 25°C, 80°C

Peak periodic forward current I_{FM} or pulsed forward current I_{Fpuls}
Peak value of the diode current during pulse operation
Parameters: pulse duration t_p, case temperature, e.g. T_{case} = 25°C, 80°C

2.3.2 Characteristics

IGBTs/ module structure

Collector-emitter breakdown voltage $V_{(BR)CES}$
Breakdown voltage between collector and emitter, gate-emitter short-circuited (V_{GE} = 0),
Parameters: collector blocking current I_C, case temperature T_{case} = 25°C

Gate-emitter threshold voltage $V_{GE(th)}$
Gate-emitter voltage above which considerable collector current will flow
Parameters: collector-emitter voltage V_{CE} = V_{GE}, collector current I_C, case temperature T_{case} = 25°C

Collector-emitter cut-off current I_{CES}
Collector-emitter blocking current with gate-emitter short-circuited (V_{GE} = 0) and collector-emitter voltage $V_{CE} = V_{CES}$
Parameter: chip temperature, e.g. T_j = 25°C and 125°C

Gate-emitter leakage current I_{GES}
Leakage current between gate and emitter with collector-emitter short-circuited (V_{CE} = 0) and at maximum gate-emitter voltage V_{GE}
Parameter: gate-emitter voltage V_{GE}, case temperature T_{case} = 25°C

Collector-emitter saturation voltage V_{CEsat}
Saturation value of collector-emitter voltage (on-state voltage drop of the active IGBT) at a specified collector current I_C (at "rated current", see chapter 2.3.3, or at maximum collector current). For PT-IGBTs V_{CEsat} will drop proportionally to the temperature within rated current range, for NPT-IGBTs, however, it will rise proportionally to the temperature.
Parameters: collector current I_C, gate-emitter voltage V_{GE}, chip temperature, e.g. T_j = 25°C and 125°C.
For calculation of forward on-state losses the following parameters are often indicated additionally in the datasheets: $V_{CE(TO)}$ (static collector-emitter threshold voltage) and r_{CE} (on-state slope resistance) of a substitutional straight line.

$V_{CEsat} = f(I_C) = V_{CE(TO)} + r_{CE} * I_C$

This means that, for calculation, the saturation voltage characteristic is approximated by means of a diode characteristic.

Forward transconductance g_{fs}
Quotient of changing collector current and gate-emitter voltage at a specified collector current I_C,
Parameters: collector-emitter voltage V_{CE}, collector current I_C ("rated current", resp.),
case temperature T_{case} = 25°C

Capacitance chip-case C_{CHC}
Capacitance between a sub-component and case base plate or heatsink potential
Parameter: case temperature T_{case} = 25°C

Input capacitance C_{iss}
Capacitance between gate and emitter with collector-emitter short-circuited for AC and gate-emitter voltage V_{GE} = 0.
Parameters: collector-emitter voltage $V_{CE,}$ measuring frequency f, case temperature T_{case} = 25°C

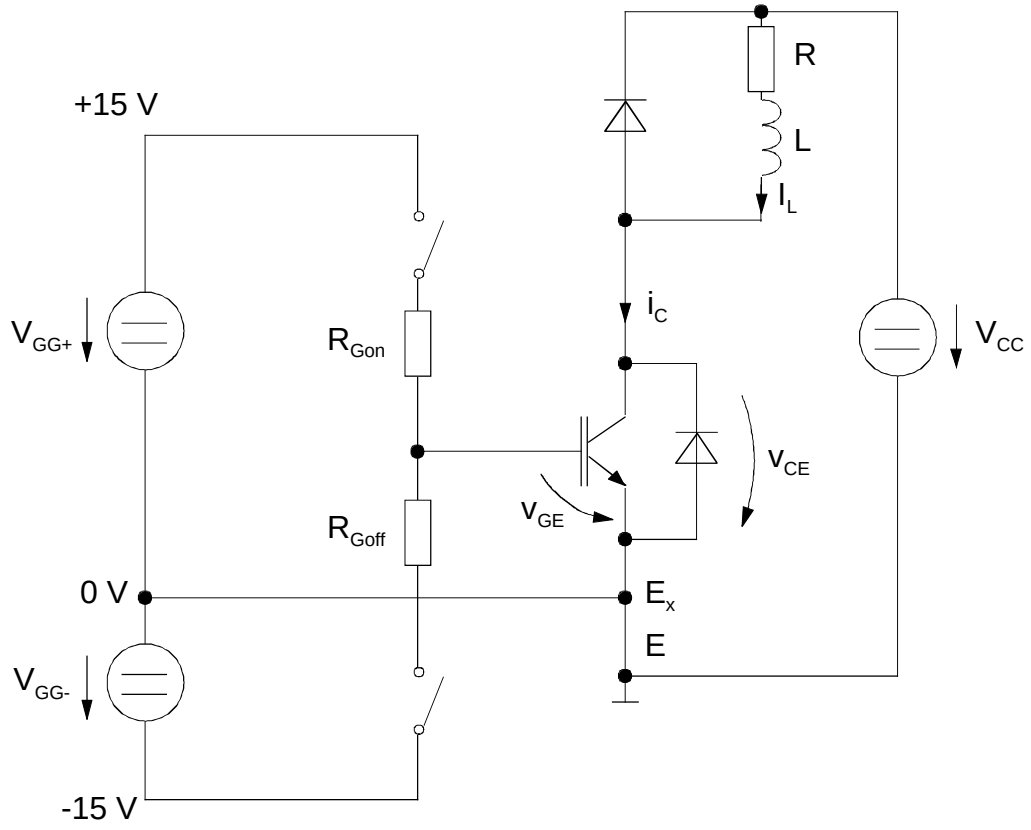
Output capacitance C_{oss}
Capacitance between collector and emitter with gate-emitter short-circuited (V_{GE} = 0).
Parameters: collector-emitter voltage V_{CE}, measuring frequency f, case temperature T_{case} = 25°C

Reverse transfer capacitance (Miller capacitance) C_{rss}, C_{mi}
Capacitance between collector and gate with collector-emitter short-circuited for AC and gate-emitter voltage V_{GE} = 0. For measuring the emitter has to be connected with the protective shield of the measuring bridge.
Parameters: collector-emitter voltage V_{CE}, measuring frequency f, case temperature T_{case} = 25°C

Parasitic collector-emitter inductance L_{CE}
Inductance between collector and emitter

Switching times
More related to practice than switching times of MOSFETs, switching times of IGBTs indicated in the datasheets are determined from a measuring circuit under ohmic-inductive load according to Figure 2.9a. The load time constant L/R is high compared to the switching frequency cycle duration T = 1/f, so that an continuous load current is generated by the load inductance.
Just as with MOSFETs, switching times of IGBTs refer to the gate-emitter characteristics during turn-on and turn-off, see Figure 2.9b.

Switching times as well as real current and voltage characteristics are determined by internal and external capacitances, inductances and resistances of the gate and drain circuit; for this reason, all indications in the datasheets and the characteristics depicted therein may only serve as a guide.



a)

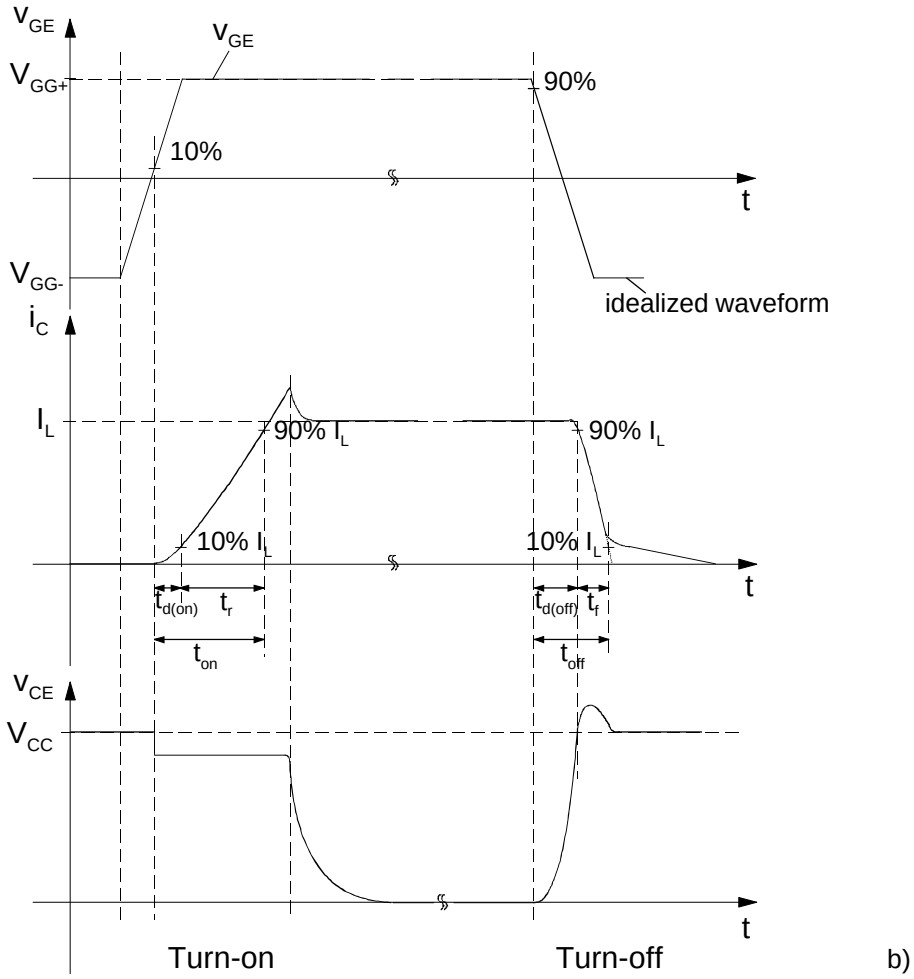


Figure 2.9 a) Measuring circuit
b) Definition of IGBT switching times under ohmic-inductive load [264],[265]

The following parameters are indicated in the datasheets relevant to switching times:
measuring circuit, collector-emitter supply voltage V_{CC}, gate-emitter control voltages V_{GG+}, V_{GG-} or V_{GE}, collector current I_C, external gate series resistors R_{Gon} ,R_{Goff} (resistance of control circuit at turn-on and turn-off), chip temperature T_j = 125°C

Turn-on delay time $t_{d(on)}$
As already mentioned, the total forward on-state current of the IGBT is to be conducted by the load inductance before turn-on.
After sudden turn-on of a positive gate-emitter control voltage, the gate-emitter voltage V_{GE} starts to rise with a time constant determined by IGBT input capacitance and gate resistance. As soon as the threshold voltage $V_{GE(th)}$ has been reached, the collector current I_C will start to rise.
The **turn-on delay time $t_{d(on)}$** is defined as the time interval between the moment when the gate-emitter voltage v_{GE} has reached 10 % of its end value, and the collector current i_C has increased to 10 % of the load current.

Rise time t_r
The **rise time t_r** is defined as the time interval following the turn-on delay time, where the collector current i_C increases from 10 % to 90 % of the load current. During this time interval most of the turn-on losses are generated in the IGBT, since a certain share of I_L is continuously conducted through the free-wheeling diode as long as the i_C-value is below load current I_L.

Therefore, the collector-emitter voltage v_{CE} will not drop significantly below the collector-emitter supply voltage V_{CC}.
The difference between V_{CC} and v_{CE} depicted in Figure 2.9b during t_r is basically determined by the transient voltage drop over the internal parasitic inductances of the commutation circuit.

The sum of **turn-on delay time $t_{d(on)}$** and **rise time t_r** is called **turn-on time t_{on}**.

As the collector-emitter voltage v_{CE} will not yet have reached its forward on-state value V_{CEsat} at the (defined) end of t_{on}, the major share of the switching losses will be generated after t_{on}.
Turn-on peak current: after the total load current I_L has been commutated to the IGBT, the free-wheeling diode will block, releasing its recovered charge Q_{rr} at the same time. Therefore, the IGBT collector current i_C will rise during reverse recovery of the free-wheeling diode (t_{rr}) by the value of the peak reverse recovery current I_{RRM} over I_L (turn-on peak current see Figure 2.10).

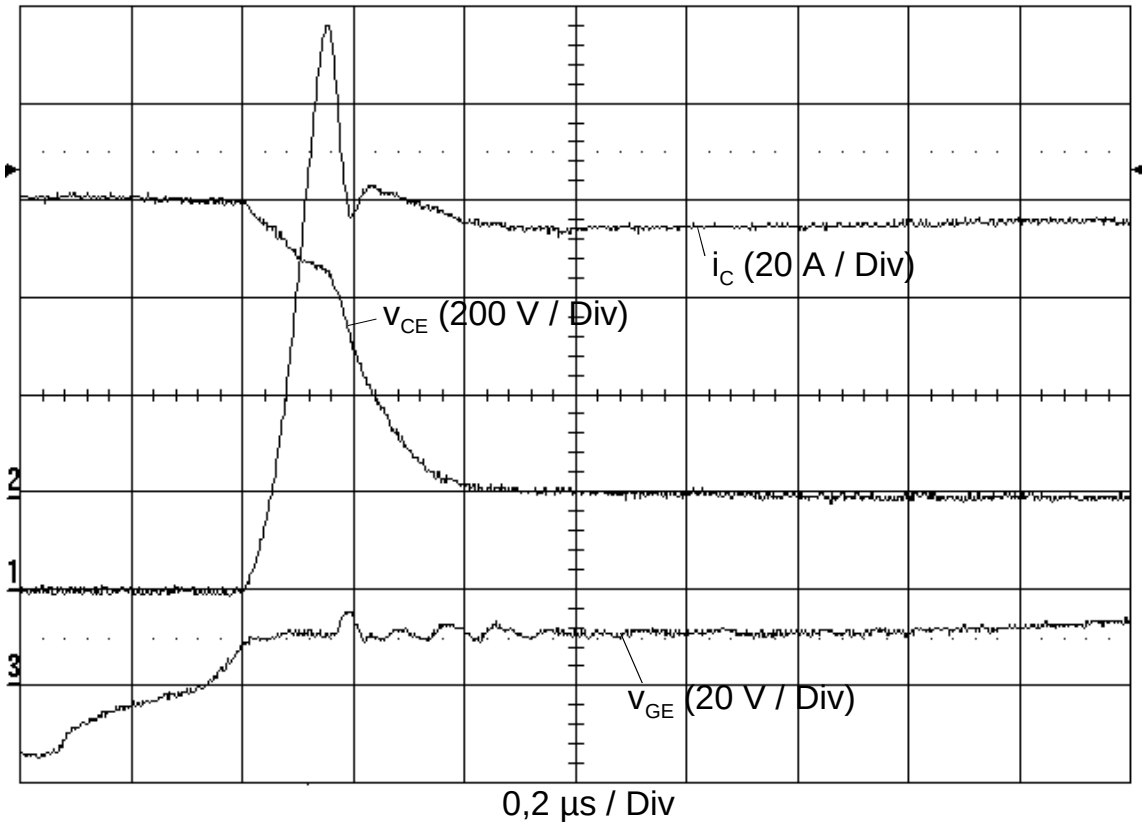


Figure 2.10 Commutation from the conducting free-wheeling diode to the IGBT (turn-on peak current) during turn-on of an IGBT

Dynamic saturation voltage: after having dropped very steeply during turn-on time, the collector-emitter voltage v_{CE} will decline relatively slowly (within µs-range) to its static value V_{CEsat}. This "dynamic saturation phase" is necessary for flooding the wide n^--zone of the IGBT with (bipolar) minority carriers (conductivity modulation).

Turn-off delay time $t_{d(off)}$
After sudden turn-off of the positive control voltage and turn-on of a negative gate-source control voltage, the gate-source voltage V_{GS} starts to decline with the time constant determined by the input capacitance of the IGBT and the gate resistance. The collector-emitter voltage v_{CE} of the IGBT begins to rise. The IGBT's collector current i_C cannot drop considerably at that time, since the free-wheeling diode is poled in reverse direction as long as V_{CC} is higher than v_{CE} and, therefore, is not able to take over load current I_L.

Due to this, the **turn-off delay time $t_{d(off)}$** for IGBTs is defined as the time interval between the moment when the gate-emitter voltage v_{GE} has dropped to 90 % of its turn-on value and the collector current has declined to 90 % of the load current value.

Fall time t_f
As soon as the collector-emitter voltage v_{CE} has exceeded the supply voltage V_{CC} during turn-off of the IGBT, the load current may commutate to the free-wheeling diode, which is poled in forward direction at that time and the collector current i_C will drop.
The **fall time t_f** is defined as the time interval, where the collector current i_C drops from 90 % to 10 % of the load current I_L.

The overshoot of v_{CE} over V_{CC} indicated in Figure 2.11 mainly results from the parasitic inductances of the commutation circuit and increases proportionally to the turn-off speed - di_C/dt of the IGBT.

The **turn-off time t_{off}** is defined as the sum of **turn-off delay time $t_{d(off)}$** and **fall time t_f**.
Since i_C will not have dropped to cut-off current level at the defined end of t_{off}, but still amounts to 10 % of the load current, the losses arising after t_{off} will still exceed the blocking losses.

Tail time t_t, tail current I_t
Other than with MOSFETs, the drastic decrease of power losses in IGBTs achieved by the injection of minority carriers in the n^--zone is realized by generation of a **tail current I_t**, shown in Figure 2.11.

The tail time t_t is not included in the turn-off time t_{off} per definition, however it contributes to a significant share of switching losses due to the collector-emitter supply voltage V_{CC} which has already been applied during that time interval.

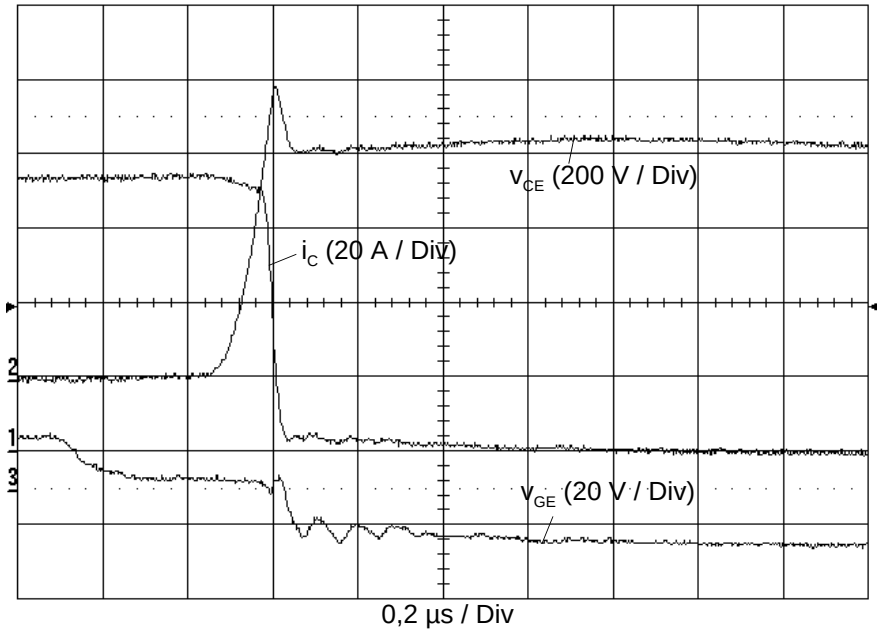


Figure 2.11 Turn-off characteristics of an NPT-IGBT

Energy dissipation during turn-on E_{on}; energy dissipation during turn-off E_{off} per cycle

The typical values of E_{on} and E_{off} of an IGBT are indicated in the diagram "turn-on/ turn-off energy E_{on}, E_{off} as a function of the collector current I_C included in the datasheet.

Power dissipation during switching may be calculated by multiplication of the switching frequency f with E_{on} or E_{off}, respectively: $P_{on} = f * E_{on}$ or $P_{off} = f * E_{off}$.

The turn-on energy dissipation E_{on} comprises the effects of the reverse peak current of the free-wheeling diode, which corresponds to the diode integrated in the power module. Energy dissipation during turn-on may be determined by integration of the power dissipation during turn-on P_{on} up to the moment when V_{CE} amounts to approximately 3 % of the collector-emitter supply voltage V_{CC}.

Apart from the power losses generated during the actually defined turn-off time $t_{off} = t_{d(off)} + t_f$, energy dissipation during turn-off also comprises the tail current losses generated during the tail time t_t up to the moment when the collector current has fallen below load current by 1 %.

Parameters: operating voltage, chip temperature T_j = 125°C, control voltages, gate series resistance.

Thermal resistance junction to case R_{thjc} per IGBT

The thermal resistance R_{thjc} describes the passage of heat between the IGBT chips (index j) and the module case (index c). It characterizes the static heat dissipation of an IGBT system within a module (mostly consisting of paralleled chips) and depends on chip size and module assembly.

The temperature difference ΔT_{jc} between chip temperature T_j and case temperature T_{case} at a constant power dissipation P is defined as follows: $\Delta T_{jc} = T_j - T_{case} = P * R_{thjc}$.

Contact thermal resistance case to heatsink R_{thch} per IGBT module

The thermal resistance R_{thch} describes the passage of heat between module case (index c) and heatsink (index h). It characterizes the static heat dissipation of an IGBT module (possibly with several IGBT switches) and depends on module size, heatsink and case surfaces, thickness and parameters of thermal layers (pastes, foils, print covers) between module and heatsink as well as on the mounting torque of the fixing screws.

The temperature difference ΔT_{ch} between case temperature T_c and heatsink temperature T_h at a constant total amount of single power dissipations P_n within the module is defined as follows: $\Delta T_{ch} = T_{case} - T_h = P_n * R_{thch}$.

Separate determination of R_{thjc} and R_{thch} is not possible for modules without base plate (e.g. SEMITOP, SKiiPPACK, MiniSKiiP). For these module, R_{thjh} is indicated per IGBT and per module. The temperature differences may be calculated in analogy.

Mechanical data

Apart from the **case construction type** mainly the following mechanical data are indicated in the datasheets:
Mounting torque M_1 of the fixing screws (minimum and maximum value) in Nm or lb.in.;
Mounting torque M_2 of the output terminals (minimum and maximum value) in Nm or lb. in.;
Weight w of the module in g;
Permissible **acceleration under vibration a** in $m*s^{-2}$.

Free-wheeling diodes

Inverse diode forward voltage (negative emitter-collector voltage) V_{EC}, V_F
Negative emitter-collector voltage drop with gate-emitter short-circuited ($V_{GE} = 0$). V_{EC} describes the forward characteristics of free-wheeling diodes, which are connected antiparallel to the IGBTs.
Parameters: forward current I_F; case temperature $T_{case} = 25°C$

Threshold voltage of the inverse diode $V_{(T0)}$
Forward slope resistance of the inverse diode r_T
With the help of threshold voltage and forward slope resistance a simplified approximation of the forward characteristic may be produced. The threshold voltage indicates the point of crossover with the voltage axis, the forward slope resistance determines the rate of rise of the characteristic.

Reverse recovery time of the inverse diode t_{rr}
Reverse recovery time of the IGBT inverse diode during free-wheeling operation, i.e. when a high collector current $-I_C = I_F$ is commutated with a high di_F/dt and a high reverse voltage $V_R = V_{CC}$.
Note: t_{rr} is very strongly dependent on the temperature (almost doubled value between 25°C and 150°C).
Parameters: forward current I_F; reverse voltage V_R, rate of fall of forward current $-di_F/dt$, chip temperature $T_j = 25°C$ and 150°C.

Recovered charge of inverse diode Q_{rr}
Recovered charge of IGBT inverse diode during free-wheeling operation, i.e. when a high collector current $-I_C = I_F$ is commutated with a high di_F/dt and a high reverse voltage $V_R = V_{CC}$.
Note: Q_{rr} is very strongly dependent on the temperature (initial value may be doubled or even increased eight-fold between 25°C and 150°C).
Parameters: forward current I_F; reverse voltage V_R, rate of fall of forward current $-di_F/dt$, chip temperature $T_j = 25°C$ and 150°C.

Thermal resistance junction to case R_{thjc} per diode
The thermal resistance junction to case R_{thjc} describes the passage of heat between diode chips (index j) and module base plate (index c).

2.3.3 Diagrams

Following the sequence of the datasheets, this chapter will give some hints concerning IGBT datasheet diagrams. In cases where the diagram concerned is detailed in other chapters, this will be referred to.

Maximum total power dissipation P_{tot} of IGBT module versus case temperature T_{case}

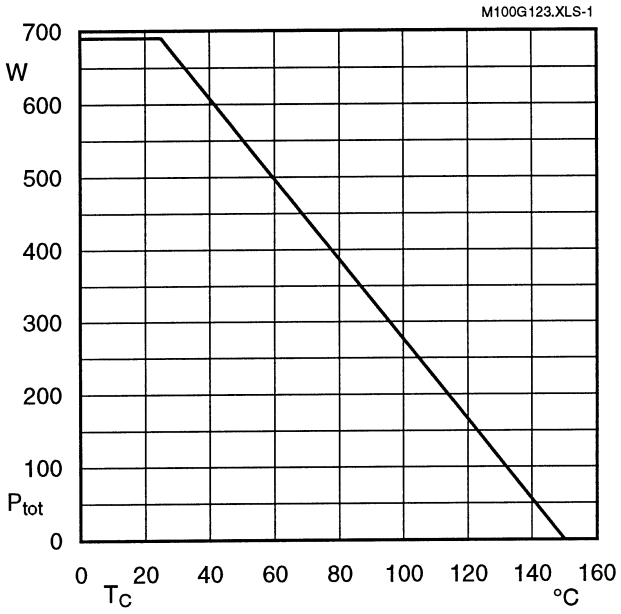


Figure 2.12 Maximum total power dissipation

Based on the maximum total power dissipation per IGBT (or per free-wheeling diode) $P_{tot(25°C)} = (T_{jmax} - 25°C)/R_{thjc}$ which is limited to $T_{case} = 25°C$ per definition, the function depicted in the diagram describes derating at a higher case temperature.

Turn-on/ turn-off energy E_{on}, E_{off} per pulse of an IGBT as function of the collector current I_C

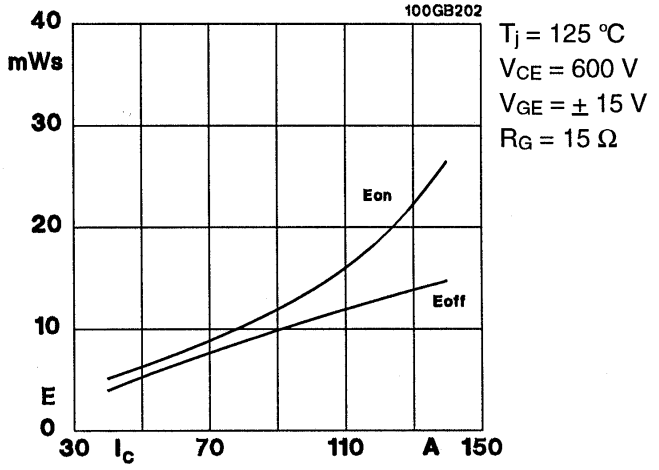


Figure 2.13 Turn-on/ -off energy dissipation as function of I_C

The turn-on/-off energies E_{on}, E_{off} determined from a measuring circuit under ohmic-inductive load are indicated versus different collector currents I_C (e.g. chip temperature T_j = 125°C, collector-emitter supply voltage V_{CC} = 600 V) with specified control parameters.
Switching losses may be determined by multiplying dissipation energy and switching frequency f:

$P_{on} = f * E_{on}$ $P_{off} = f * E_{off}$.

E_{on} and E_{off} are indicated for IGBT at rated current (I_c@ T_{case} = 80°C) in the characteristic values of the datasheet.

Turn-on and turn-off energy E_{on}, E_{off} per pulse of an IGBT as function of the gate series resistors R_G (R_{Gon}, R_{Goff})

see chapter 3.5.2

Maximum safe operating area during switch operation (SOA)

As explained in chapter 1.2.3 the IGBT has to manage an almost rectangular characteristic i = f(u) between V_{CC} and I_L in case of hard switching.
The SOA (**S**afe **O**perating **A**rea)-diagrams indicate to what extent this may be realized during different operations without risk of destruction:

- SOA for switching, on-state and single pulse operation
- RBSOA (Reverse Biased SOA) for periodic turn-off
- SCSOA (Short Circuit SOA) for non-perdiodic turn-off of short circuits (chapter 3.6.2)

The SOA is limited by the following parameters:

- maximum collector current (horizontal limit);
- maximum collector-emitter voltage (vertical limit);
- maximum power dissipation or chip temperature (diagonal limits) see Figure 2.14;

Maximum safe operating area during pulse operation (SOA)

Figure 2.14 shows the maximum curve $I_C = f(V_{CE})$ during switching and on-state for different pulse durations t_p at a double logarithmic scale.

It is important that the maximum ratings are valid at a case temperature T_c = 25°C and for single pulses, which will not heat the IGBT over the maximum chip temperature T_j = 150°.
Although the lowest of the depicted diagonals represents the hyperbola of the maximum stationary power losses P_{tot}, IGBT modules may only touch the linear characteristic area with approximately V_{CE} > 20 V or V_{GE} < 9 V during switching operation. Analogous operation over a longer period of time is not permitted, since asymmetries due to variation among the chips as well as negative temperature coefficients of the threshold voltages might cause thermal instability.

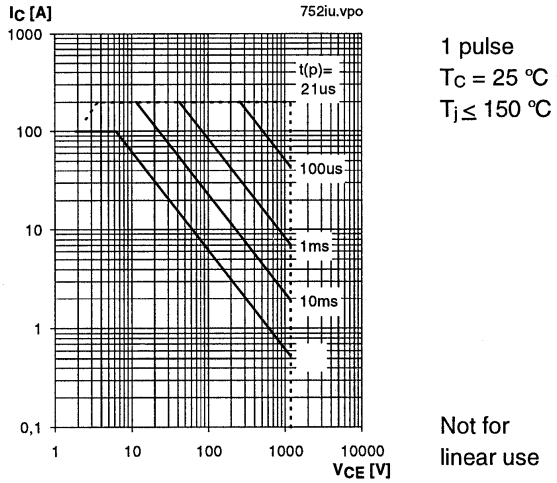


Figure 2.14 Maximum safe operating area $I_C = f(V_{CE})$ during pulse operation (SOA)

Turn-off safe operating area

Figure 2.15 shows the turn-off safe operating area of an IGBT.

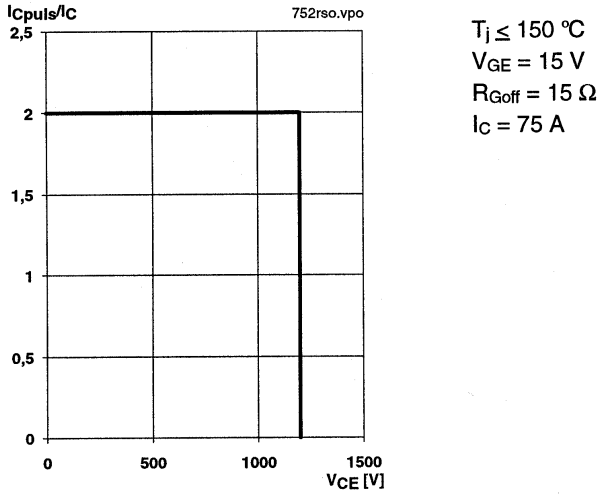


Figure 2.15 Turn-off safe operating area (RBSOA)

During periodic turn-off the IGBT may effect a hard turn-off of I_{CM}@80°C = T_C for T_{jmax} and defined driver parameters, provided that v_{CE} (chip) has reached V_{CES}-level (influence of parasitic inductances and driver parameters, see chapters 3.4.1 and 3.5.2).

Safe operating area at short circuit

see chapter 3.6.2

Derating of collector current versus case temperature

see chapter 2.6; analogous to Figure 2.23b

Forward output characteristic $I_C = f(V_{CE})$

Figure 2.16 shows the output characteristics for T_j = 25°C and 125°C (typical values) with parameter V_{GE}, also see chapters 1.2.2.2 and 2.6.

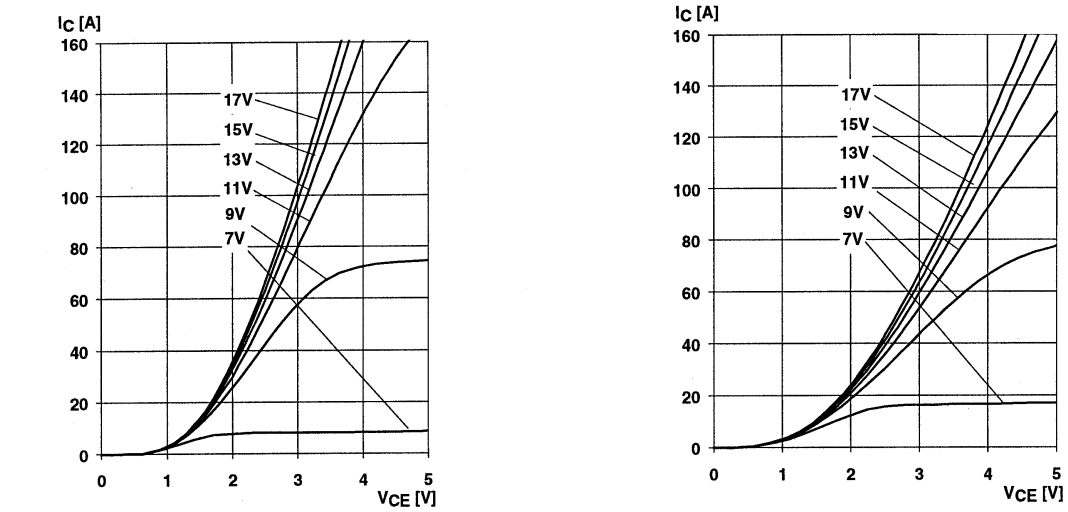


Figure 2.16 Typical IGBT output characteristic $I_C = f(V_{CE})$ with paramter V_{GE}
a) T_j = 25°C b) T_j = 125°C

Transfer characteristic $I_C = f(V_{GE})$

The transfer characteristic (Figure 2.17) describes the behaviour of the IGBT within the active area at V_{CE} = 20 V and t_p = 80 µs (linear operation). The collector current is coupled with the gate-emitter voltage via transfer transconductance: $I_C = g_{fs} * (V_{GE}-V_{GE(th)})$.

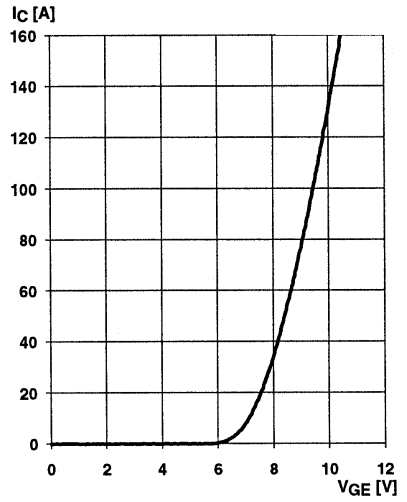


Figure 2.17 Typical transfer characteristic $I_C = f(V_{GE})$

Gate charge characteristic

see chapter 1.2.3

Internal capacitances versus collector-emitter voltage

see chapter 1.2.3

Switching times versus collector current

Figure 2.18 shows typical dependencies of switching times $t_{d(on)}$ (turn-on delay time), t_r (rise time), $t_{d(off)}$ (turn-off delay time) and t_f (fall time) on the collector current I_C during hard switching of inductive loads.

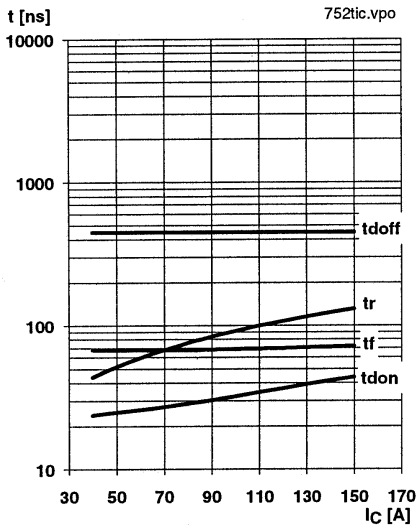


Figure 2.18 Typical dependency of switching times on collector current (inductive load)

The slightly overproportional increase of t_r verifies that di_C/dt does not increase to the same extent as I_C when the collector current rises.

Switching times versus gate resistor

see chapter 3.5.2

CAL diode forward characteristic

see chapter 1.3.1.1

Diode turn-off energy dissipation

Figure 2.19 demonstrates the dependency of the diode turn-off energy E_{offD} on the diode current I_F conducted before turn-off, and on the turn-on speed of the IGBT determined by gate resistance R_G, during current commutation between free-wheeling diode and IGBT (hard switching).

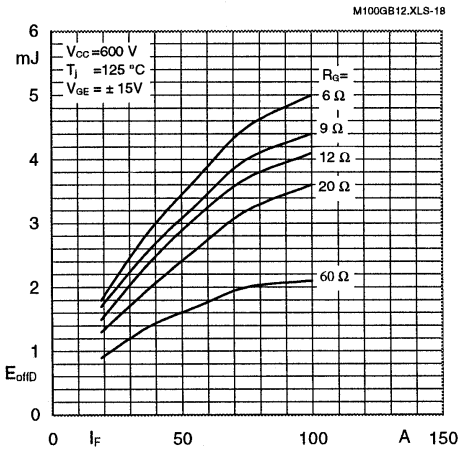


Figure 2.19 Diode turn-off energy dissipation E_{offD} versus collector current I_C and gate resistance R_G

As expected, the diode turn-off losses increase with the forward current as well as with the rate of rise of commutation current due to a simultaneous rise of storage charge and reverse current amplitude (see chapter 1.3.1.3).

Transient thermal impedances of IGBT and free-wheeling diode

see chapter 3.2.2.3

Free-wheeling diode reverse recovery current as function of forward on-state current

Figure 2.20 shows typical values of the peak reverse recovery current I_{RRM} versus forward current I_F and di/dt determined by the gate resistance $R_G = R_{Gon}$.

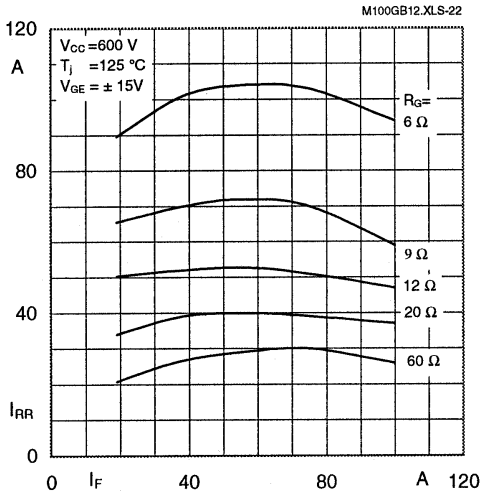


Figure 2.20 Typical peak reverse recovery current I_{RRM} of free-wheeling diode versus I_F and R_G

As expected, the peak reverse recovery current is higher, the faster the IGBT is switched on (low R_{Gon}).
At first, the reverse recovery current will increase together with rising forward current. If high collector currents are applied, the share of charge carriers in the CAL-diode drift area, which already re-combine during commutation, will increase with the duration of commutation; therefore, I_{RRM} will again drop in the high current range.

Free-wheeling diode reverse recovery current as function of di_F/dt

Figure 2.21 depicts the typical dependency of the free-wheeling diode reverse recovery current I_{RRM} on di/dt, determined by control of the given gate resistances $R_G = R_{Gon}$ of the IGBT on the measuring conditions indicated.

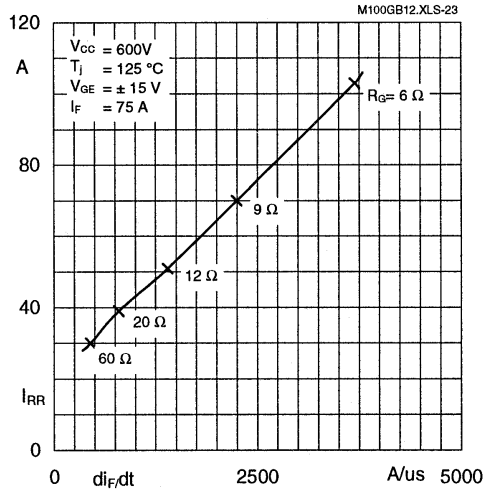


Figure 2.21 Typical free-wheeling diode reverse recovery current I_{RRM} versus di/dt and R_G

The reverse recovery current increases almost linearly to di/dt.

Free-wheeling diode recovered charge as function of di_F/dt

Figure 2.22 shows the typical dependency of the free-wheeling diode recovered charge Q_{rr} on di/dt for different collector currents I_C. In addition, the gate resistances $R_G = R_{Gon}$ have been entered which determine the given di/dt on the measuring conditions indicated.

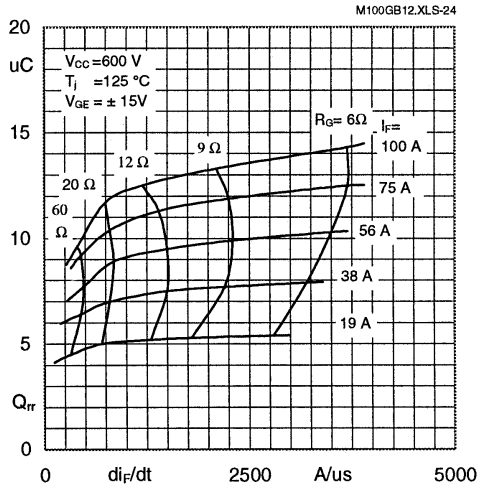


Figure 2.22 Typical free-wheeling diode recovered charge versus di/dt, R_G and I_C

Just like the reverse recovery current, the free-wheeling diode recovered charge will rise together with the collector current and di/dt. The rate of rise will be more distinct for high collector currents than for the low current range.

Rated collector current at short circuit as a function of gate-emitter voltage and temperature

see chapter 3.6.2

2.4 Special parameters for MiniSKiiPs

Apart from IGBTs and diodes for inverters and brake choppers diodes (or thyristors) for input rectifiers are also integrated in the MiniSKiiP.
Supplementary to forward and blocking characteristics (maximum ratings, characteristics), the follwing parameters are specified for MiniSKiiPs:

Rectifier diode surge forward current I_{FSM}

Peak value of a sinusoidal wave 50 Hz, which the diode is able to withstand without being damaged in the case of breakdown, if this does not occur too often.

Rectifier diode peak load integral $\int i^2dt$

Reference parameter for the selection of fuses to be calculated as follows: $\int i^2dt = I_{FSM}^2 * T/4 = 5*10\text{-}3s * I_{FSM}^2$ (@ f = 50 Hz)

Resistance/ temperature coefficient of the temperature sensor

Features of current sensors

2.5 Special parameters for SKiiPPACKs

SKiiPPACK datasheets have to include for example:
- static/dynamic maximum ratings and characteristics of IGBT and free-wheeling diode chips;
- thermal characteristics (including heatsink);
- indications on isolation voltage of module and of all potential separations;
- indications on threshold values of protective function;
- input level, output performance and delay times of the driver and
- indications on features related to mechanical stress and climate conditions.

Therefore, SKiiPPACK datasheets are much more complex, although, on the other hand, all indications concerning the dependency of parameters on different driver conditions may be ignored.

2.6 Temperature dependency of static and dynamic characteristics of power modules

Almost all electrical characteristics of IGBTs, power MOSFETs and free-wheeling diodes are more or less dependent on the chip temperature.
The following table reflects the characteristic tendencies of the most important component parameters at rising temperature (<: rises; <<: rises steeply; >: falls; -: no notable temperature dependency).
The special features marked with * are only valid for PT-IGBTs.
For dimensioning in practice, the parameters marked with **!**, which will be detailed later on, are of main importance due to their distinct dependency on the temperature. For the temperature dependency of the parameters of free-wheeling diodes please refer to the explanations under chapter 1.3.

Parameter	**MOSFET**	**IGBT**	**Free-wheeling diode**
Avalanche breakdown voltage	<	<	<
Blocking current, blocking power dissipation	<	<	<
Turn-on resistance/forward on-state voltage, forward power dissipation	<<!	<(>*)!	>
Turn-on time/energy dissipation during turn-on	<	<	-
Turn-off time/energy dissipation during turn-off	<	<(<<*)!	<<
Threshold voltage	>	>	>
Forward transconductance	>	>	-

For the interpretation of the parameters indicated in the datasheets it should be taken into consideration that many ratings for power MOSFETs and IGBTs are related to a case temperature of 25°C and have still to be converted to the maximum operating temperature by means of other indicated parameters.
This goes mainly for the maximum permissible drain or collector current I_D, I_{DM}, I_C, I_{CM} and the maximum power dissipation P_{tot} or P_D, respectively, which have to be reduced to ratings under realistic operating conditions as described in chapter 3.1.2.
The required current reduction is determined by the forward and blocking power dissipations which are also temperature-dependent, as well as by the switching losses.

The fact that *blocking current and blocking power dissipation* will increase by factor 3...6 between 25°C and 125°C is of only minor importance for dimensioning, because the blocking power dissipation contributes to only a small share of total power dissipation.

In contrast to this, the forward on-state temperature dependency is of major importance, which, therefore, shall be examined separately for the single components:

Power MOSFET

Figure 2.23 shows the increasing on-resistance $R_{DS(on)}$ of a power MOSFET and the resulting over-proportional derating of the continuos drain current I_D at higher temperatures with an example.

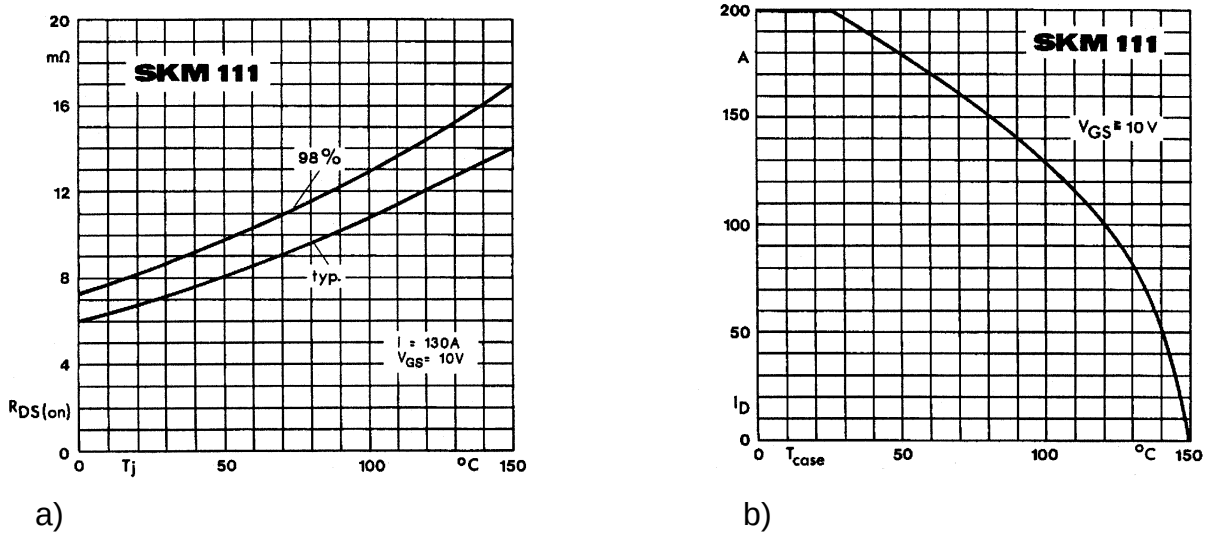


Figure 2.23 Forward on-state behaviour of a 100 V power MOSFET versus temperature
a) On-resistance $R_{DS(on)}$ b) Continuous drain current I_D derating

$R_{DS(on)}$ is doubled within the operating temperature range of 25...150°C; at T_{case} = 80°C only 75 % of the maximum drain current I_D can be utilized even under static conditions.
On the other hand, the positive temperature coefficient of the forward on-state voltage offers advantages such as simplified paralleling ability and high resistivity during hard switching.

IGBT

The various concepts of IGBTs (PT/NPT, see chapter 1.2.1) also differ in their thermal behaviour.
This is explained in Figure 2.24 with the basic characteristic of the collector-emitter saturation voltage V_{CEsat} over the collector current I_C at a chip temperature of 25°C and 125°C.

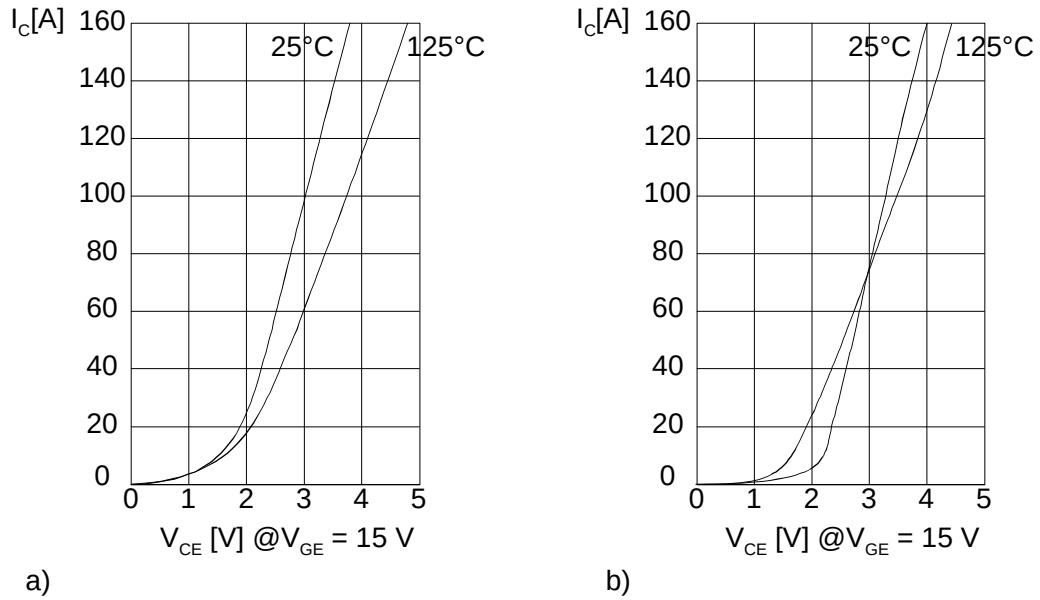


Figure 2.24 Forward characteristics of IGBTs
a) SEMITRANS NPT-IGBT 100A@25°C b) PT-IGBT 100A@25°C

The temperature coefficient of the forward on-state voltage V_{CEsat} of the NPT-IGBT is positive for the whole current (approx. 8 mV/K at I_C@25°C). The temperature coeffcient of V_{CEsat} of the PT-IGBT, however, is negative for the actually utilized forward current range and rises to zero only when rated current has been approximated.
The resulting consequences for NPT-IGBTs compared to PT-IGBTs are higher forward power dissipation on the one hand, and a better current symmetry on the other hand (homogeneous temperature spreading/ ruggedness, unselected paralleling ability).

The I_C-derating characteristic versus temperature analogous to Figure 2.22b is included in the IGBT-datasheets as well.

As already mentioned, MOSFET and IGBT *switching times and switching losses* will also increase when the temperature rises.
However, since dimensioning for “hot“ chips has to be done in practice anyway, most ratings included in the current datasheets are taken at 125°C .

In this respect, another difference between NPT- and PT-IGBTs should be referred to (Figure 2.25, see chapters 1.2.1 and 1.2.3)

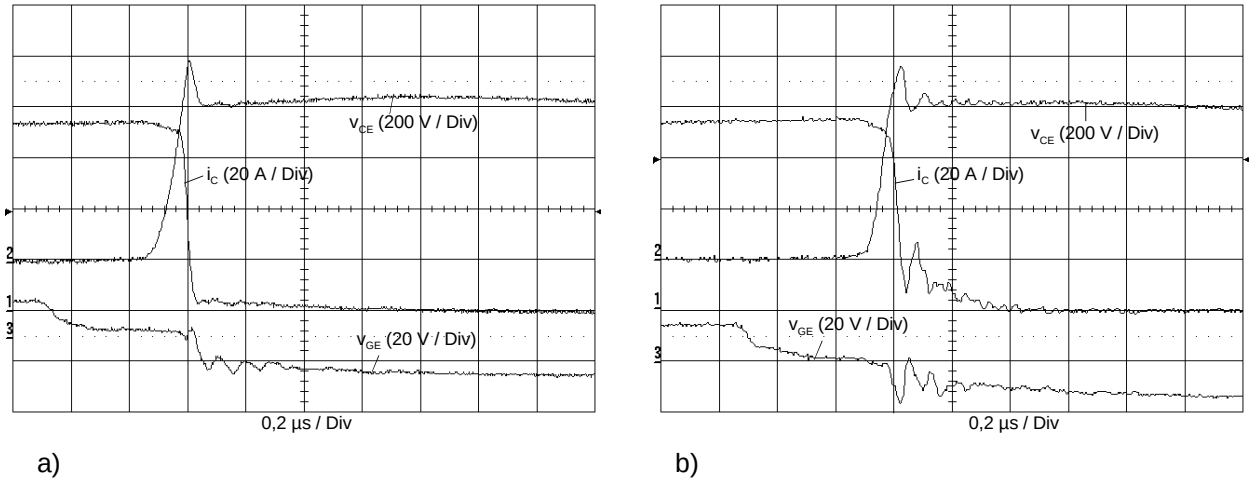


Figure 2.25 Turn-off behaviour of IGBTs
a) SEMITRANS NPT-IGBT b) PT-IGBT

The tail current I_t generated during turn-off will increase together with the temperature. Whereas the tail current of an NPT-IGBT will have risen by almost 100 % at 125°C compared to 25°C (Figure 2.25a), the tail current of PT-IGBT (Figure 2.25b) will be almost tripled within this temperature range. This results in clearly reduced switching losses of NPT-IGBTs at high temperatures compared to PT-types.

The minor temperature dependency of *threshold voltage and forward transconductance* has practically no importance for switching operation. But it is a basic restriction to linear operation of power modules.

2.7 Reliability

Reliability, i.e. maintaining the promised characteristics over a defined period of time, is one of the most important quality features of power modules.
On the one hand, power modules are outstanding for their high electrical and thermal efficiency; on the other hand, premature failure may cause danger, direct and consequent damage and, last but not least, high costs.
Reliability is very difficult to express due to comparably small lots, often extreme long life requirements (10...30 a) and complex test specifications, but may be defined by

- exact control of all influences on production processes (built-in reliability),
- reliability testing under conditions very close to the application in order to discover typical failure mechanisms,
- testing of the components within the system and control of the most important parameters. [231]

Some selected tests for power modules are shown in the following without going into details of the extensive EN ISO 9001 quality assurance system, based on which SEMIKRON is able to grant a 2 year TQM warranty on all its power semiconductors.

The following standard tests are being carried out for release and re-qualification of MOSFET and IGBT modules still to become finalised by further, individual product-specific reliablity testing:

Test	Standards	Test conditions
High temperature blocking voltage (HTRB)	DIN 41749, IEC 147-4	1.000h, V_{DSmax}, V_{CEmax}, T_{jmax}
Hot gate stress	DIN 45930, CECC 50000-4, 5.2	1.000h, V_{GSmax}, V_{GEmax}, T_{jmax}
High temperature storage	DIN 45930, CECC 50000-4, 4.3	1.000h, T_{stgmax}
Low temperature storage		1.000h, T_{stgmin}
Humidity temperature blocking	DIN 45930, CECC 50000-4, 4.3	1.000h, 85°C, 85 % relative humidity. V_{CE}, V_{DS} = 0.8 V_{CEmax}, V_{DSmax} ; ≤ 80 V
Temperature cycling	DIN IEC 68-2-14-test Na	100 temperature cycles T_{stgmax}/T_{stgmin}
Power cycling	DIN 41794, IEC 147-4	20.000 cycles, ΔT_j=100 K
Solder temperature	DIN IEC 68-2-20, test Tb	260±5°C, 10±1 s
Solderability	DIN IEC 68-2-20, test Ta	235±5°C, aging 3
Vibration/ acceleration	acc.to DIN IEC 68-2-6,test F_c	5 g

The following failure criteria according to standard MIL-STD-19500 are valid:

Gate-drain-/gate-emitter leakage current I_{GSS}, I_{GES}: > ± 20 nA or >100 % of initial rating

Zero gate voltage drain current or
collector-emitter cut-off current I_{DSS}, I_{CES}: > ± 100 µA or >100 % of initial rating (max. 2x of specified max. rating)

On-resistance/forward voltage $R_{DS(on)}$, V_{CEsat}: > 120 % of initial rating

max. change of threshold voltage $V_{GS(th)}$, $V_{GE(th)}$: >± 20 % of initial rating

Thermal resistance junction to case R_{thjc}: > 120 % of initial rating

Isolation test voltage V_{isol}: < specified maximum rating

Figure 2.26 and Figure 2.27 show examples for test procedures depicting measuring circuits and procedures for temperature cycling and power cycling.

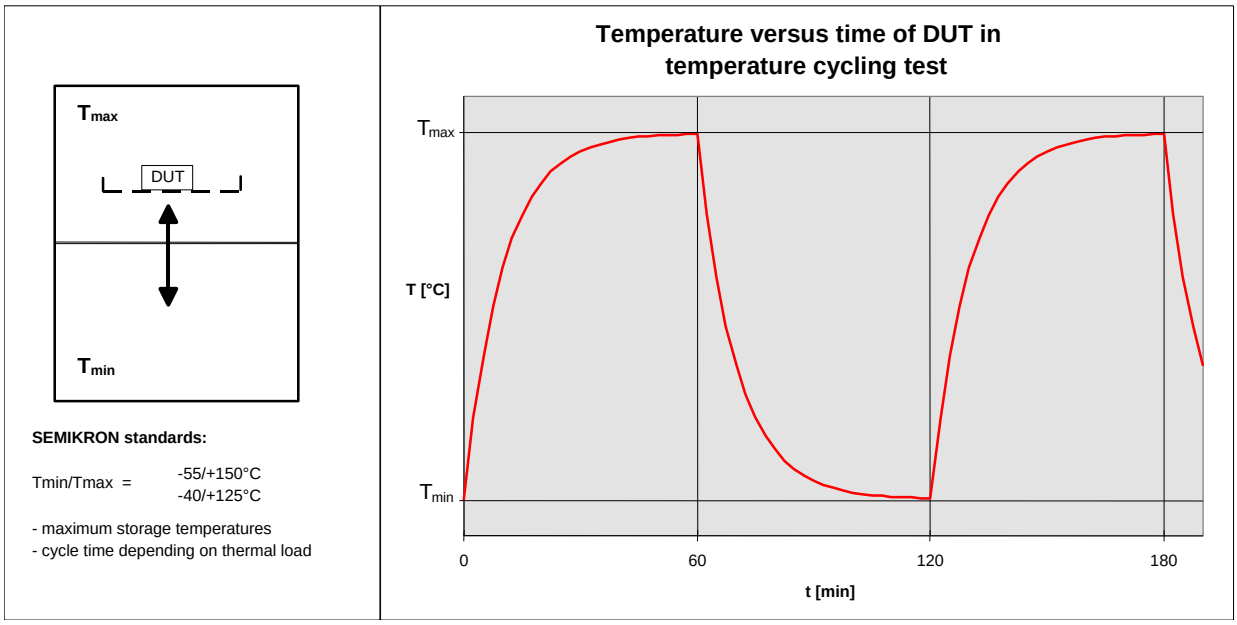


Figure 2.26 Temperature cycling: measuring circuit and measuring procedure

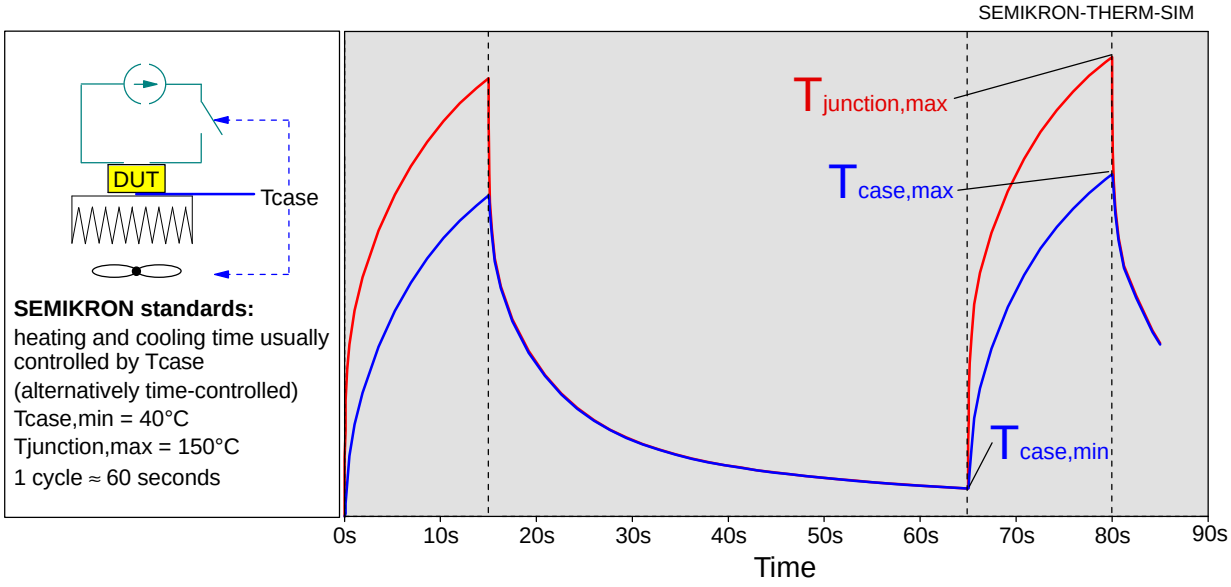


Figure 2.27 Power cycling: measuring circuit and measuring procedure

Principal characteristics of power modules related to reliability may be checked by means of temperature and power cycling testing, see also chapter 1.4.2.4. Therefore, these tests are of decisive importance for the qualification of modules.

3 Hints for application

3.1 Dimensioning and selection of MOSFET, IGBT and SKiiPPACK modules

The selection of power modules for any static or short-term (overload) operating conditions of a concrete application is subject to the consideration of

- voltage capacitance,
- current carrying capacity under realizeable cooling conditions and with reference to the switching frequency and
- safe operating areas (SOA).

Under no circumstances that might occur during any static or dynamic operation must the maximum ratings for blocking voltage (except for avalanche-proof MOSFETs), peak current, junction temperature and safe operating area (see chapter 2.7) indicated in the datasheets be exceeded. The same goes for the limit values of module case parameters (e.g. isolation voltage, vibration strength, climate persistence, assembly instructions).
For the sake of high reliability and long life, modules have to be designed for managing a specified number of switching cycles, which usually go along with considerable temperatures cycling. (Chapters 1.4.2.4 and 3.2.3).
Furthermore, „serious“ dimensioning will not presuppose total thermal utilization of the semiconductors to their maximum ratings $T_{j(max)}$ (e.g. 150°C) in order to keep a margin for theoretically unforeseeable cases and to be able to fall back upon the static and dynamic characteristics taken at a maximum of 125°C and guaranteed by the manufacturers.
As already explained in chapter 2.6, the most important characteristics of power modules will deteriorate when the temperature rises. For this and other reasons, the determination of the maximum operating temperature has to be paid special attention to.

3.1.1 Forward blocking voltage

Since most power modules are applied in DC-voltage links, which are AC-voltage supplied via single-phase or three-phase rectifier bridges, the blocking voltages of universally applied IGBTs (600 V, 1200 V, 1700 V) are adjusted to common line voltage levels; the same goes for highly blocking MOSFET-modules.
Therefore, firstly a rough selection is made from line voltage (control angle 0° for controlled rectifiers) V_N or no-load direct voltage V_{di} as follows:

V_N/V	rectification	V_{di}/V	V_{DSS}, V_{CES}/V
24	B2	22	50
48	B2	44	100
125	B2	110	200
200...246	B2	180...221	500, 600
400...460	B6	540...621	1200
575...690	B6	777...932	1700
...1000...	B6	1500	3300

Afterwards, it has to be checked whether on condition of utmost voltage capacitance, i.e.
- maximum stationary input voltage (nominal voltage + line voltage tolerance, e.g. 15 %),
- transient line overvoltage, as far as it has not yet been reduced by line filters, DC-link capacitors and circuits on the DC-side (suppressor diodes, snubbers, varistors),
- turn-off overvoltage $V_d + \Delta V$

the maximum module voltage will be exceeded with

$$\Delta V = L_\sigma * I_{max}/t_f$$

with parameters as follows:

L_σ: parasitic commutation inductance, see chapters 1.4.2.5 and 3.4.2,

I_{max}: maximum turn-off collector or drain current (mostly with active short-circuit turn-off, see chapter 3.6),

t_f: fall time of collector or drain current.

Here, special attention has to be paid to the fact that the maximum rating for V_{DSS}/V_{CES} indicated in the datasheets is related to the characteristics of the transistor chips and not to the „dynamic" terminal behaviour of the module. The internal module inductance L_{CE} also indicated in the datasheets (e.g. 20...30 nH) therefore corresponds to a share of L_σ; the voltage applied to the chips will exceed the voltage to be taken at the terminals by $L_{CE} * I/t_f$ during turn-off. This is expressed by a diagram in the SEMITRANS MOSFET datasheets, which explains the derating of the permissible drain-source voltage at the terminals versus the rate of fall of the drain current $di_D/dt \approx I_D/t_f$ (Figure 3.1).

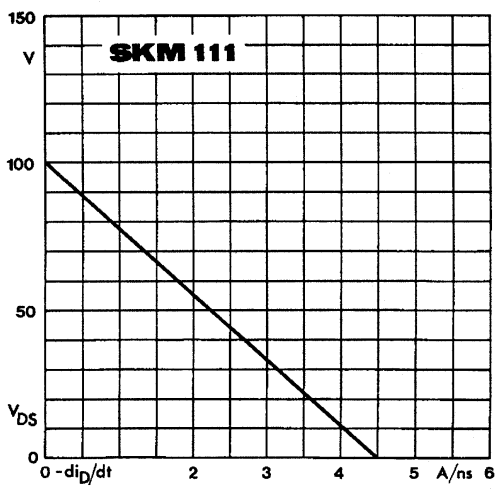


Figure 3.1 Drain-source voltage V_{DS} derating of a SEMITRANS MOSFET-module SKM 111 A versus drain current rate of fall di_D/dt

3.1.2 Forward current

The maximum continuous drain or collector currents I_D or I_C, respectively, indicated in the datasheets as typical currents for module designation and as maximum ratings may be calculated for a stationary fully controlled transistor at a case temperature T_{case} of, for example, 25°C or 80°C according to the following formula

$$I_D = \sqrt{\left(T_{j(max)} - T_{case}\right) / \left(R_{DS(on)} \cdot R_{thjc}\right)} \qquad \text{(MOSFET-module)}$$

or $I_C = (T_{j(max)} - T_{case})/(V_{CEsat} * R_{thjc})$ (IGBT-module)

For modules without base plate T_h will replace T_{case} and R_{thjh} will replace R_{thjc}. The ratings for $R_{DS(on)}$ and V_{CEsat} have been taken at a maximum chip temperature $T_{j(max)}$.
These indications are only intended to give an orientation aid, since under real operating conditions switching and (low) blocking losses will occur additionally to the forward on-state losses, the case temperature will differ and the static maximum ratings of $R_{DS(on)}$ or V_{CEsat} will not be reached during the whole turn-on procedure.
At a given case temperature (25°C, 80°C), the peak current values for I_{DM} or I_{CM} are specified for single pulses with a pulse duration of 1 ms and, at the same time, are designating the maximum current ratings for periodic turn-on and turn-off (SOAR).

Therefore, the utilizeable forward current is determined
- mainly by the total power dissipation of the transistors and free-wheeling diodes of a power module and the chip temperatures within the transistors and free-wheeling diodes arising under specific cooling conditions (R_{thca}), which must not exceed $T_{j(max)}$ (chapter 3.2.2),
- by the limits of the maximum safe operating area, see chapters 2.2 and 2.3. To avoid exceeding the limit values during hard turn-on under ohmic-inductive load, the amount of load current and reverse recovery current of the free-wheeling diode must not exceed I_{DM} or I_{CM}, see Figure 3.2. Due to the reasons mentioned in chapter 1.3.1.3 a compromise has to be found between turn-on speed of the transistor (increase of turn-on losses!) and conductable load current in most cases.

Further restrictions in practice have possibly to be accepted resulting from the characteristics of active overcurrent protection in the driver (see chapter 3.5).

3.1.3 Switching frequency

Figure 3.2 shows the measured turn-on and turn-off behaviour of a power MOSFET and an IGBT module for one specific operating point.

Apart from the characteristics for v_{DS} or v_{CE} and i_D or i_C also the instantaneous power dissipation p(t) had been determined by multiplication of instantaneous current and voltage values; the integral of p(t) reflects the total MOSFET and IGBT losses over the whole period.

To determine total power dissipation of the power module, the losses of the free-wheeling diode(s) within the module have to be added to the losses in the transistor, see chapter 3.2.1.

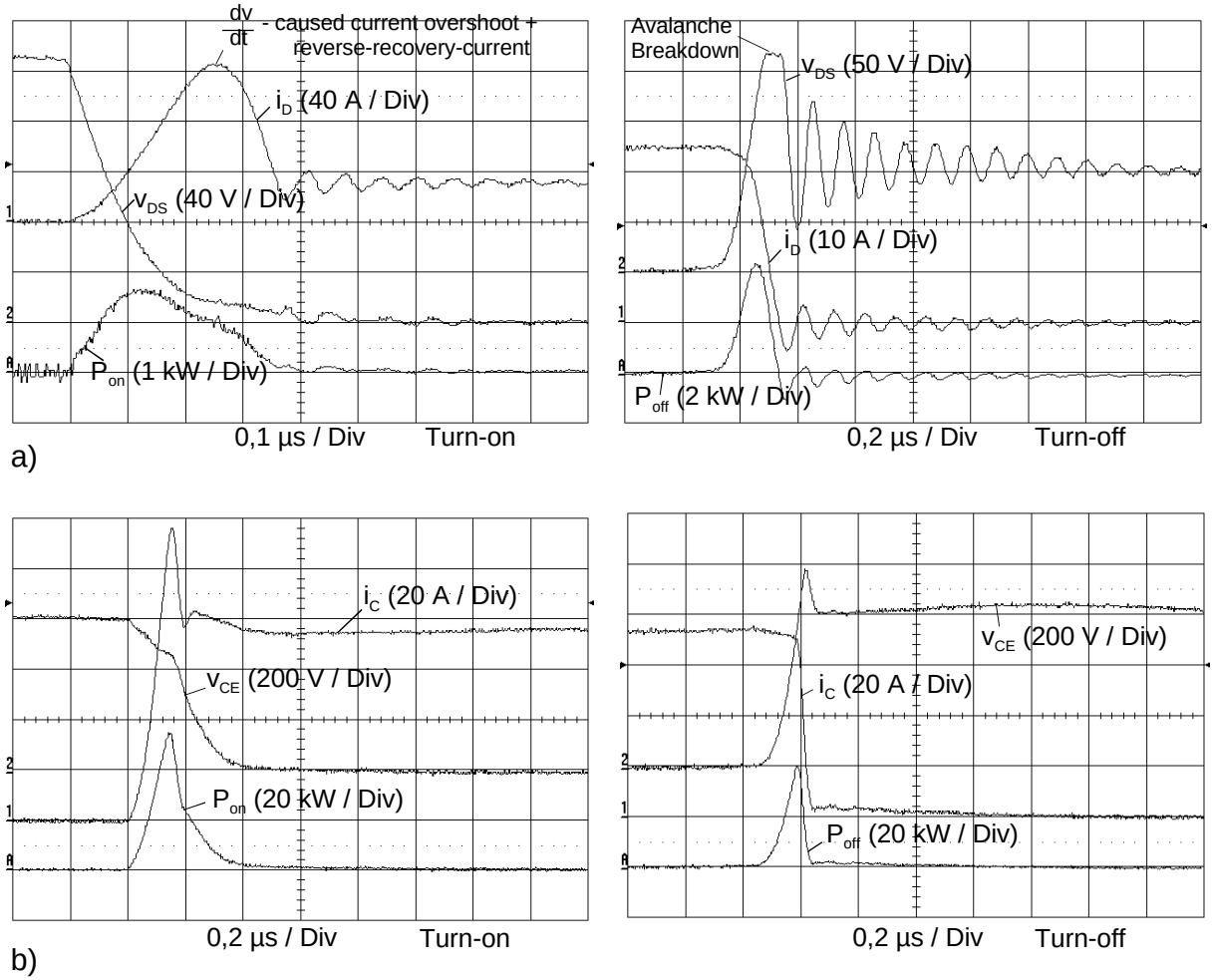


Figure 3.2 Measured switching processes (hard turn-on and turn-off under ohmic-inductive load)
a) Power-MOSFET module b) IGBT module

For explanations on quality features of current and voltage characteristics please refer to the remarks on Figure 1.11 in chapter 1.2.3.

The actual limits to the switching frequency are set by the switching losses, because they are increasing proportionally to the frequency.
Other terminations may be set by the transistor turn-on and turn-off delay times $t_{d(on)}$, $t_{d(off)}$, the reverse recovery times of the free-wheeling diodes, the driver output power which increases proportionally to the frequency and the minimum turn-on, turn-off or dead times necessary for driver, interlocking, measuring, protection and monitoring functions, see chapter 3.5.1...3.5.4.
If switching losses are to be shifted to passive networks (snubbers) or overvoltages are to be limited by snubbers, the recharge time of such networks required after low-loss switching has to be considered as deadtime, see chapters 3.6 and 3.8.

Switching times of MOSFET and IGBT power modules are within the range of some 10 ns to some 100 ns. Especially when high operating voltages and hard switching processes are involved, the theoretically reachable maximum switching frequency cannot be utilized in most cases, since the maximum switching speed is often determined by

- the turn-off speed, limited by the permissible switching overvoltage and

- the turn-on speed, limited by the permissible peak current (load current + reverse recovery current of the free-wheeling diode depending on di/dt).

Moreover, transistor dv/dt and di/dt values, which are prone to be very steep within the high power range, might cause electromagnetic interferences and problems due to dv/dt in certain loads (machines).
Therefore, an optimized compromise between the requirements resulting from the application (e.g. frequency out of range of audibility), switching times/ losses, power dissipation and EMC-features has to be looked for when determining switching frequency and switching times.

These are the standard values for switching frequencies with standard modules, optimal technical utilization provided:

for hard switching:	MOSFET-modules	low-voltage	up to 250 kHz
		high-voltage	up to 100 kHz
	IGBT-modules	600 V	up to 30 kHz
		1200 V	up to 20 kHz
		1700 V	up to 10 kHz
		3300 V	up to 3 kHz
for soft switching:	MOSFET-modules	low-voltage	up to 500 kHz
		high-voltage	up to 250 kHz
	IGBT-modules		up to 150 kHz

Higher switching frequencies can be realized with modules specially designed for fast switching.

3.2 Thermal behaviour

3.2.1 Balance of power losses

3.2.1.1 Single and total power losses

Introductory remarks

All explanations in chapter 3.2 refer to IGBT modules. All considerations and calculations are applicable to MOSFET modules in analogy, provided all designation indices corresponding to MOSFETs are exchanged.
The following explanations are focused on hard switching converters connected to a DC-voltage-link.

In power electronics, IGBTs as well as diodes are operated mainly as switches, taking on various static and dynamic states in cycles. In any of these states, one power dissipation or energy dissipation component is generated, which heats the semiconductor and adds to the total power dissipation of the switch. Therefore, the maximum junction temperature T_j= 150°C (for silicon components) given by the manufacturer has to be obeyed at any time of operation of the converter when using power semiconductors.

Figure 3.3 shows a survey of the possible single power dissipations during switch operation.

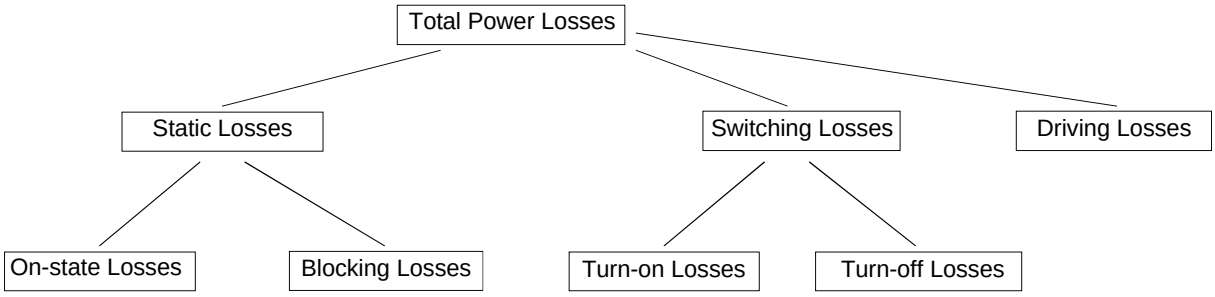


Figure 3.3 Single power losses of power module switches

IGBT

Because they are only contributing to a minor share of the total power dissipation, forward blocking losses and driver losses may usually be neglected.

On-state power dissipations ($P_{fw/T}$) are dependent on:
- load current (over output characteristic $v_{CEsat} = f(i_C, v_{GE})$),
- junction temperature,
- duty cycles.

For given driver parameters, the turn-on and turn-off power dissipations ($P_{on/T}$, $P_{off/T}$) are dependent on:
- load current,
- DC-link voltage,
- junction temperature,
- switching frequency.

IGBT total power losses: $\mathbf{P_{tot/T} = P_{fw/T} + P_{on/T} + P_{off/T}}$

Free-wheeling diode:

Because they are only contributing to a minor share of the total power dissipation, reverse blocking power dissipations may usually be neglected. Schottky diodes might be an exception due to their high-temperature blocking currents.
Turn-on power dissipations are caused by the forward recovery process. As for fast diodes, this share of the losses may mostly be neglected as well.

On-state power dissipations ($P_{fw/D}$) are dependent on:
- load current (over forward characteristic $v_F = f(i_F)$),
- junction temperature,
- duty cycles.

For given driver parameters of the IGBT commutating with the diode, turn-off power dissipations ($P_{off/D}$) are dependent on:
- load current,
- DC-link voltage,
- junction temperature,
- switching frequency.

Total diode power losses: $\mathbf{P_{tot/D} = P_{fw/D} + P_{off/D}}$

Hybrid power module with n IGBTs and m diodes

Total module power losses: $\mathbf{P_{tot/M} = (n * P_{tot/T}) + (m * P_{tot/D})}$

3.2.1.2 Power losses of a step-down converter

Figure 3.4 shows the circuit diagram of a step-down converter with characteristics generated under ohmic inductive load.

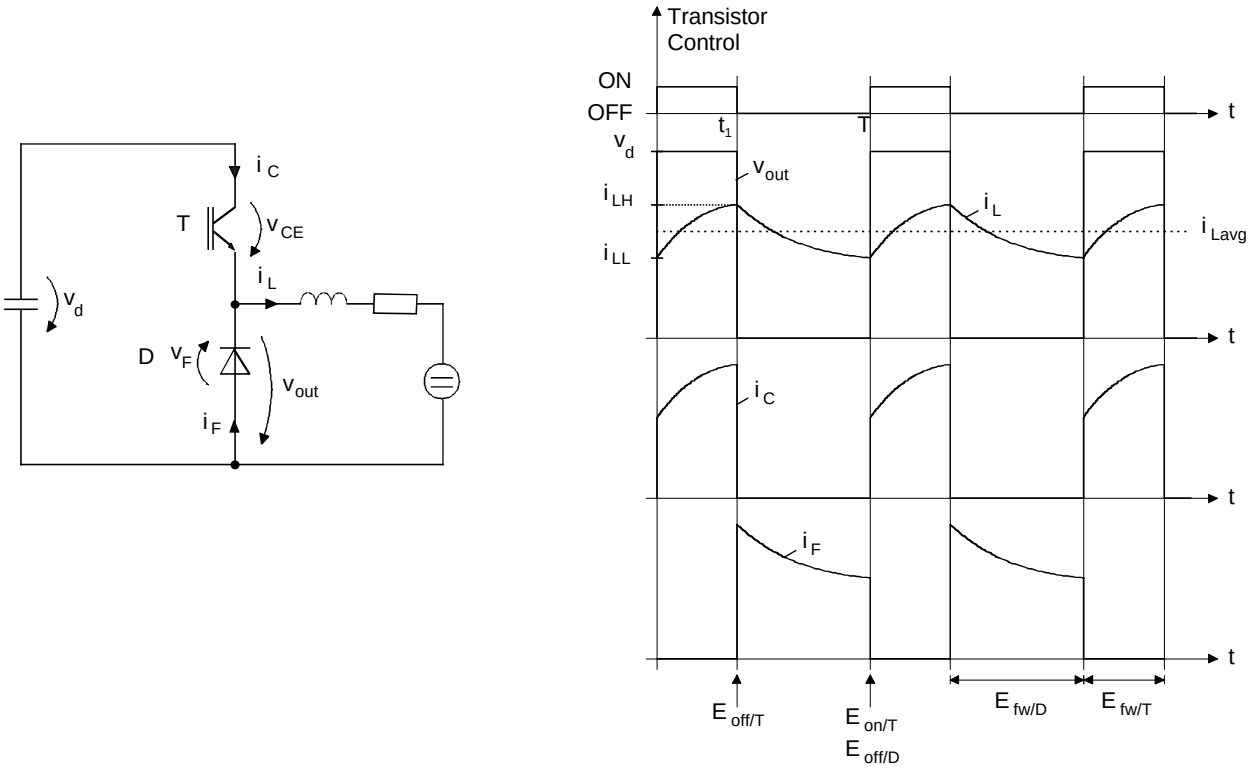


Figure 3.4 Step-down converter under ohmic-inductive load

During the steady state of the circuit, power dissipations at a certain operation point may be calculated as follows:

IGBT

Turn-on power dissipation: $P_{on/T} = f_s * E_{on/T} (v_d, i_{LL}, T_{j/T})$
Turn-off power dissipation: $P_{off/T} = f_s * E_{off/T} (v_d, i_{LH}, T_{j/T})$

Foward power dissipation: $$P_{fw/T} = \frac{1}{T}\int_0^{t_1} i_C(t) \cdot v_{CE}(t)\, dt$$

Neglecting the load current ripple will result in:

$$P_{fw/T} = i_{Lavg} * v_{CEsat} (i_{Lavg}, T_{j/T}) * (t_1/T)$$
$$= i_{Lavg} * v_{CEsat} (i_{Lavg}, T_{j/T}) * D_T$$

D_T = transistor duty cycle
i_{Lavg} = average load current

Free-wheeling diode

Turn-off power dissipation: $P_{off/D} = f_s * E_{off/D} (v_d, i_{LL}, T_{j/D})$

Forward power dissipation: $P_{fw/T} = \frac{1}{T}\int_{t_1}^{T} v_F(t) \cdot i_F(t)\, dt$

Neglecting the load current ripple will result in:

$$P_{fw/D} = i_{Lavg} * v_F (i_{Lavg}, T_{j/D}) * (1-D_T)$$
$$= i_{Lavg} * v_F (i_{Lavg}, T_{j/D}) * (D_D)$$

D_D = diode duty cycle

The calculation of IGBT and diode forward power dissipation is based on an ideal duty cycle (neglecting the share the switching time contributes to the total cycle duration).
Selected ratings for energy dissipations during switching as well as for the IGBT and diode forward voltage drop are indicated in the datasheets (see chapter 2).

3.2.1.3 Power losses in pulsed voltage source inverters/rectifiers with sinusoidal currents

Basic circuit: Figure 3.5 shows ideal characteristics of an inverter phase for a sinusoidal modulation according to the sinusoidal pulse-width modulation.

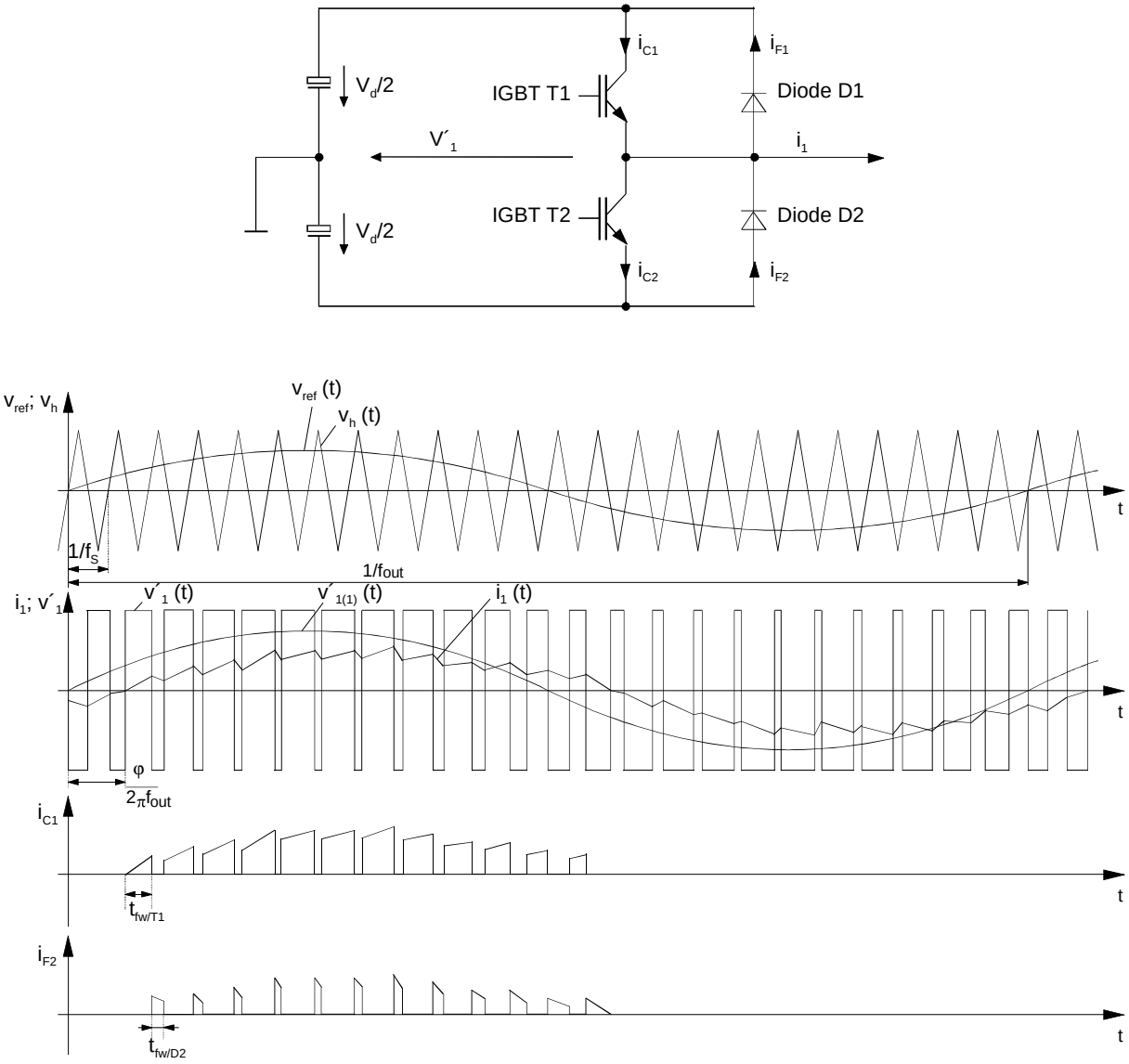


Figure 3.5 Converter phase with sinusoidal modulation according to sinusoidal pulse-width modulation

In the sinusoidal pulse-width modulation the pulse pattern is generated by comparison of a reference voltage v_{ref} to an auxiliary control voltage v_h, whereby the fundamental frequency of the AC-parameters f_{out} is determined by the reference voltage and the switching or pulse frequency of the switches f_s by the auxiliary control voltage.

The intersections of reference and auxiliary control voltage are the basis for commutation times in the converter phase.

If $\hat{v}_{ref} \leq \hat{v}_h$, this is called linear modulation mode of the inverter.

The following explanations refer to the linear modulation mode. Furthermore, it is presupposed that the fundamental frequency of the AC-parameters is exceeded by the pulse frequency by far.

Voltage utilization of the converter may be expressed by the degree of modulation m. It indicates the ratio between fundamental harmonics amplitude of the AC-voltage and 50 % of the DC-link voltage. In case of a pure sinusoidal reference voltage, the degree of linear modulation will be $0 \leq m \leq 1$.

The phase shift between the fundamental harmonics of AC current and voltage is described by the angle φ.
The current and voltage characteristics for IGBTs and diodes, which are time-shifted, will turn out to be identical due to the symmetrical structure of the inverter circuit. Therefore, it is enough to consider just one IGBT (here T1) and one diode (here D2) with reference to the calculation of power dissipation (the result is then multiplied by the corresponding number of IGBTs/ diodes integrated in the inverter).
In contrast to the calculations under chapter 3.2.1.2 duty cycle, load current and junction temperature are not constant under static operation, but vary depending on the fundamental frequency of the AC side (e.g. 50/60 Hz). This means that switching and forward power dissipations of IGBTs and diodes are subject to temporal variability and require a extensive calculation of system power losses.
Consequently, exact results cannot be produced with greatly simplified calculation procedures.

Two calculation possibilities are to be introduced in the following.

1. Approximation of component characteristics by polynominal equations (detailed in [194])

In this calculation procedure, the dependencies of transistor and diode forward on-state voltages on load current and junction temperature as well as of transistor and diode switching energy dissipations on load current, DC-link voltage and junction temperature are approximated by polynominal equations of the type $y = f(x) = A + Bx + Cx^2$. For this, the available component parameters have to be taken from the datasheets or determined by simple pulse converter test circuits, which, however, requires considerable effort.
The following set-up of the polynominal equations may be done by using conventional curve-fitting software.
The coefficients A-C of a following equations comprise the determined dependencies of the parameters.

Accordingly, equations 3.1-3.4 may be set up to calculate the average energy dissipation.
The following simplifications have been presupposed:
- transistor and diode switching times are neglected,
- temporally constant junction temperatures (permissible if f_{out} = ..50 Hz),
- linear modulation of the converter,
- neglecting the switching frequency ripple of the AC-current.

Forward power dissipation

Including forward characteristic approximation of IGBT and diode according to y = A + Bx and considering the temperature coefficients of the forward on-state voltages, results in the following equations:

IGBT T1:

$$P_{fw/T1} = \left(\frac{1}{2} - \frac{t_{dead}}{T_S}\right) \cdot \left(\frac{A_{fw/T}}{\pi} \cdot \hat{i}_1 + \frac{B_{fw/T}}{4} \cdot \hat{i}_1^{\,2}\right) + m \cdot \cos\varphi \cdot \left(\frac{A_{fw/T}}{8} \cdot \hat{i}_1 + \frac{B_{fw/T}}{3\pi} \cdot \hat{i}_1^{\,2}\right) \qquad (3.1)$$

Diode D2:

$$P_{fw/D2} = \left(\frac{1}{2} + \frac{t_{dead}}{T_S}\right) \cdot \left(\frac{A_{fw/D}}{\pi} \cdot \hat{i}_1 + \frac{B_{fw/D}}{4} \cdot \hat{i}_1^{\,2}\right) - m \cdot \cos\varphi \cdot \left(\frac{A_{fw/D}}{8} \cdot \hat{i}_1 + \frac{B_{fw/D}}{3\pi} \cdot \hat{i}_1^{\,2}\right) \qquad (3.2)$$

Figure 3.6 explains the influence of switching deadtime t_{dead} on forward energy dissipations (t_{dead} determines the effective duty cycles) with the example of a 1200 V/50 A-IGBT-module. Especially if high pulse frequencies are involved, the arm-interlock-deadtime t_{dead} has to be considered in the calculation of the average power forward dissipation.

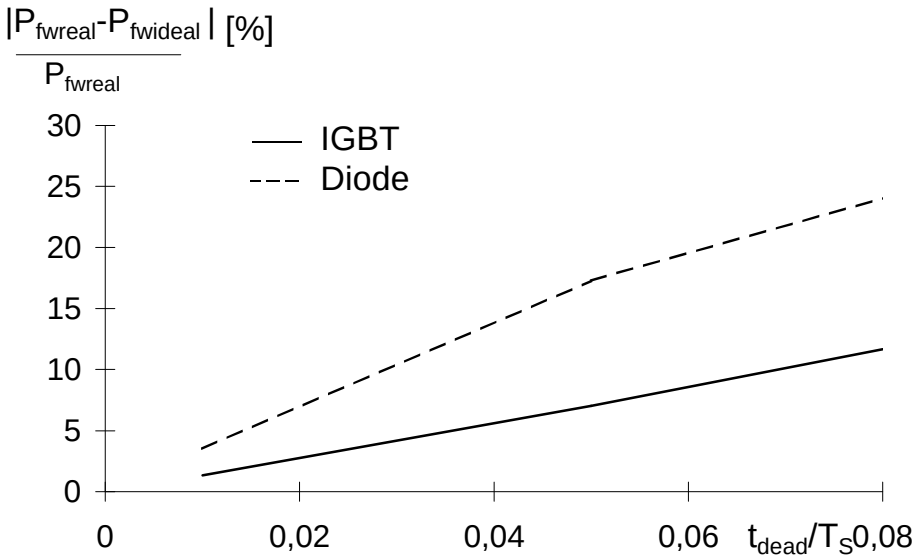


Figure 3.6 Forward power dissipations versus switching deadtimes (i_{1eff} = 25 A; m = 0.8; cos φ = 0.8)

Switching losses

The following equations result from the approximation of the dependency of switching losses on the current according to $y = Bx + Cx^2$ in consideration of temperature and voltage coefficients of the switching losses:

IGBT T1:
$$P_{on+off/T1} = f_s \cdot \hat{i}_1 \left(\frac{B_{on+off/T}}{\pi} + \frac{C_{on+off/T}}{4} \cdot \hat{i}_1\right) \qquad (3.3)$$

Diode D2:
$$P_{off/D1} = f_s \cdot \hat{i}_1 \left(\frac{B_{off/D}}{\pi} + \frac{C_{off/D}}{4} \cdot \hat{i}_1\right) \qquad (3.4)$$

Figure 3.7 shows one result of this calculation method with the example of a 1200 V/50 A-IGBT-dual module in an inverter.

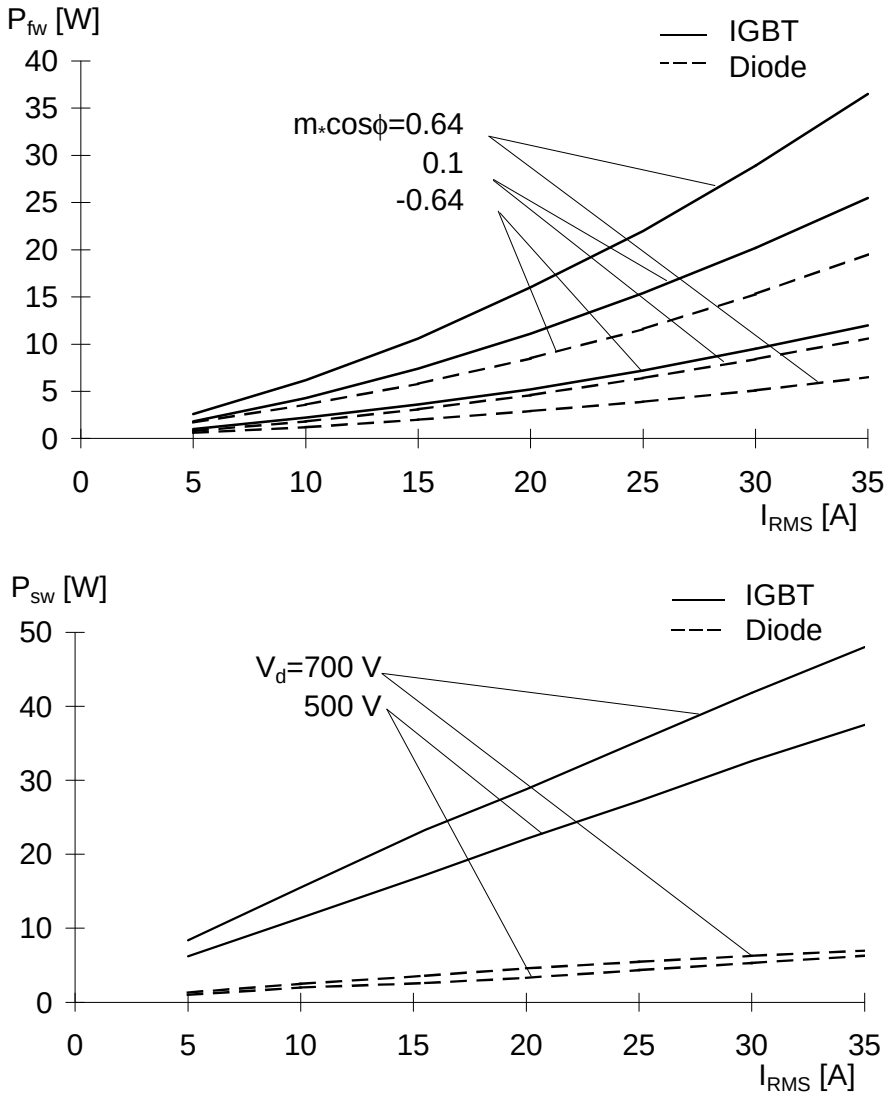


Figure 3.7 a) Forward power dissipations (t_{dead} = 5 µs, T_j = 125°C)
b) Switching losses (f_s = 10 kHz, T_j = 125°C)

The product of m*cos φ determines how the total power dissipation is divided up on IGBT and diode (see also chapter 1.3.1.4).

m*cos φ = 0.64	represents an operating point in inverter mode (motor load)
m*cos φ = 0.1	represents an operating point in motor starting mode
m*cos φ = -0.64	represents an operating point in rectifier mode

The procedure for calculation of IGBT and diode power dissipation described above shows very exact results, however the determination of parameters requires great efforts.
Therefore, the following greatly simplified calculation mode to produce a rough calculation can be recommended.

2. Simplified, linear approach [274]

Assumptions:
- transistor and diode switching times as well as switching interlocking times are neglected,
- temporally constant junction temperatures (permissible if f_{out} = ..50 Hz.),

- linear modulation of the converter,
- neglecting switching frequency ripple of the AC current (sinusoidal current),
- $f_s >> f_{out}$.

Forward on-state power dissipation:

IGBT T1:

If the output characteristics are linearized with y = A + Bx, the temporal dependency of the saturation voltage v_{CEsat} may be expressed as follows:

$$v_{CEsat}(t) = V_{CE0} + r_{CE} \cdot i_C(t) = V_{CE0} + r_{CE} \cdot \hat{i}_1 \sin \omega t$$

with: V_{CE0} = threshold voltage of the output characteristic with $i_C = 0$
r_{CE} = on-state resistance of the IGBT (rate of rise of the output characteristic)

Considering the sinusoidal dependency of duty cycles versus time, the forward power dissipation of IGBT T1 may be calculated according to

$$P_{fw/T1} = \frac{1}{2}\left(\frac{V_{CE0}}{\pi} \cdot \hat{i}_1 + \frac{r_{CE}}{4} \cdot \hat{i}_1^{\,2}\right) + m \cdot \cos\varphi \cdot \left(\frac{V_{CE0}}{8} \cdot \hat{i}_1 + \frac{r_{CE}}{3\pi} \hat{i}_1^{\,2}\right) \qquad (3.5)$$

Diode D2:

If the output characteristics are linearized with y = A + Bx, the temporal dependency of the foward on-state voltage v_F may be expressed as follows:

$$v_F(t) = V_{F0} + r_F \cdot i_F(t) = V_{F0} + r_F \cdot \hat{i}_1 \sin \omega t$$

with: V_{F0} = threshold voltage of the forward characteristic with $i_F = 0$
r_F = on-state resistance of the diode (rate of rise of the output characteristic)

Considering the sinusoidal dependency of duty cycles versus time, the forward power dissipation of diode D2 may be calculated according to

$$P_{fw/D2} = \frac{1}{2}\left(\frac{V_{F0}}{\pi} \cdot \hat{i}_1 + \frac{r_F}{4} \cdot \hat{i}_1^{\,2}\right) - m \cdot \cos\varphi \cdot \left(\frac{V_{F0}}{8} \cdot \hat{i}_1 + \frac{r_F}{3\pi} \hat{i}_1^{\,2}\right) \qquad (3.6)$$

Switching losses

IGBT T1:

Provided that the energy dissipation during switching is linearly dependent on the collector current, the total power dissipation of an IGBT may be calculated with

$$P_{on+off/T1} = \frac{1}{\pi} \cdot f_s \cdot \left[E_{on/T}\left(\hat{i}_1\right) + E_{off/T}\left(\hat{i}_1\right)\right] \qquad (3.7)$$

Equation 3.7 is actually based on the assumption that the IGBT switching losses generated during one sine half-wave are about identical to the switching losses generated if an equivalent direct current is applied, which would correspond to the average value of the sine half-wave.

IGBT switching losses are approximately convertible linearly to other DC-link voltages.

Diode D2:
Provided that the energy dissipation during turn-off is linearly dependent on the diode current, the total power dissipation of a diode may be calculated with:

$$P_{off/D2} = \frac{1}{\pi} \cdot f_s \cdot E_{off/D}\left(\hat{i}_1\right) \tag{3.8}$$

This equation is also based on the assumption that the diode switching losses generated during one sine half-wave are about identical to the switching losses generated, if an equivalent direct current is applied, which would correspond to the average value of the sine half-wave.

Diode switching losses are approximately convertible linearly to other DC-link voltages.

The results rendered by the explained simplified calculation process are sufficient for estimating the expected power dissipation during converter operation mode in practice.
The decisive advantage that is offered to the user is that all necessary parameters can be taken directly from the corresponding module datasheets.

3.2.2 Calculation of the junction temperature

3.2.2.1 General hints

The calculation of junction temperatures is based on the simplified thermal equivalent block diagram of Figure 3.8.
The designations used for transistor and diode are related to those in Figure 3.5.
The equivalent block diagram is restricted to one transistor and its commutating diode in a power module, i.e. to those two components through which the load current is conducted during one sine half-wave (here T1 and D2). The equivalent block diagram for T2 and D1 can be drawn up in analogy.

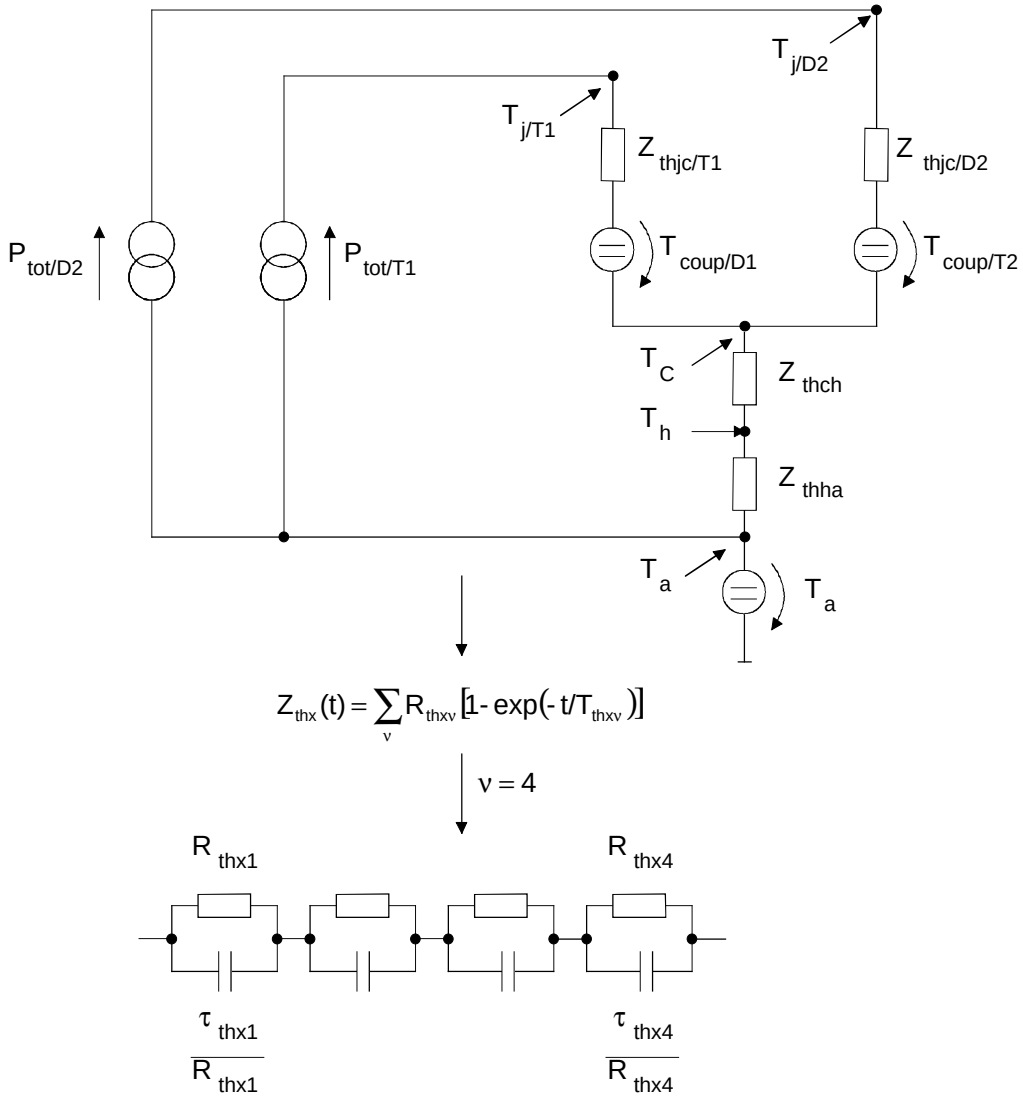


Figure 3.8 Simplified thermal equivalent block diagram of IGBT and free-wheeling diode in a power module

Explanation of designations:

P_{tot}	Total power dissipation within transistor and free-wheeling diode
T_j	Junction temperatures
Z_{thjc}	Thermal impedance from junction to module case
T_c	Case temperature
Z_{thch}	Thermal impedance from module case to heatsink
T_h	Heatsink temperature
Z_{thha}	Thermal impedance from heatsink to ambient temperature (see chapter 3.3)
T_a	Ambient temperature

Transistors and inverse diodes are soldered on a common copper plate in a power module. Therefore, the elements $T_{coup/D1}$ and $T_{coup/T2}$ stand for the thermal coupling of T1 and D2 with their corresponding antiparalleled elements D1 and T2, which becomes effective especially at low fundamental frequencies.
Exact determination of this coupling effect is subject to extensive thermal simulation of the module structure [194]. Therefore, this is usually neglected in simplified calculation processes.

If transistor and free-wheeling diode are integrated in the same module, a common heatsink and case temperature may be presumed for simplification.
If this simplifaction is no more permissible for high-power single switches, the values for Z_{thch} have to be entered separately for transistor and diode.

Efficient thermal parameters between case and heatsink are also dependent on the following factors: quality of the module base plate, contact pressure between module and heatsink, thermal paste, surface quality of the heatsink. Please pay attention to the data and recommendations given by the manufacturers (see chapter 1.4.2.2).

For computer-aided simulation of the temporal behaviour of the junction temperature thermal impedances may be divided up into a chain circuit of R-C components (see Figure 3.8).
As a special service to the customer, SEMIKRON offers parameters of 4-6 R-C components for determining the Z_{thjc} of power modules in the databook. Parameters of the cooling systems are also available on request (see chapter 3.3.6).

Following the equivalent block diagram of Figure 3.8, the characteristics of the junction temperatures of transistor and diode versus time can be calculated according to the following equations based on the case temperature:

$$T_{j/T1}(t) = T_C + T_{coup/D1} + P_{T1}(t) \cdot \sum_{\nu=1}^{n} R_{th\nu/T1}\left[1 - \exp\left(-t/\tau_{th\nu/T1}\right)\right] \qquad (3.9)$$

$$T_{j/D2}(t) = T_C + T_{coup/T2} + P_{D2}(t) \cdot \sum_{\nu=1}^{n} R_{th\nu/D2}\left[1 - \exp\left(-t/\tau_{th\nu/D2}\right)\right] \qquad (3.10)$$

Often only the average junction temperatures and their ripples are decisive for the thermal layout of converters. Exemplary calculations for typical loads are explained in the following chapters.

3.2.2.2 Junction temperature during short-time operation

Short-time operation allows for higher currents to be conducted in the power semiconductors than indicated in the datasheets for permanent operation. However, the highest junction temperature generated under the given conditions should not exceed the maximum rating of $T_j = 150°C$.
The junction temperature can be calculated using formulas 3.9 and 3.10 in chapter 3.2.2.1.

Examples:

Single power dissipation pulse

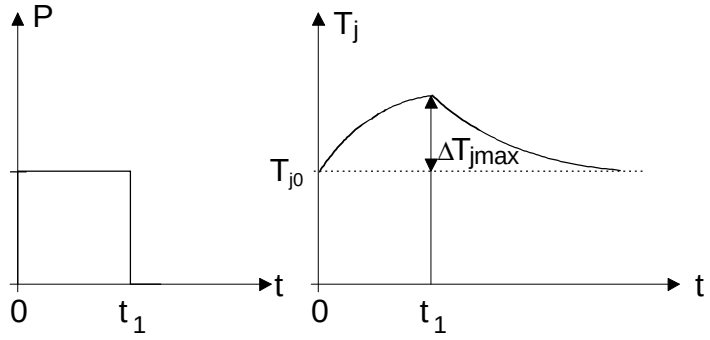


Figure 3.9 Power dissipation and junction temperature of single power dissipation pulse versus time

Maximum value of the junction temperature alteration at t_1:

$$\Delta T_{jmax} = \Delta T_j(t_1) = P \cdot \sum_{\nu=1}^{n} R_{th\nu}\left[1 - \exp\left(-t_1/\tau_{th\nu}\right)\right] \tag{3.11}$$

Junction temperature during cooling periode:

$$\Delta T\left(t > t_1\right) = P \cdot \sum_{\nu=1}^{n} R_{th\nu}\left[1 - \exp\left(-t/\tau_{th\nu}\right)\right] - P \cdot \sum_{\nu=1}^{n} R_{th\nu}\left[1 - \exp\left(-\left(t - t_1\right)/\tau_{th\nu}\right)\right] \tag{3.12}$$

These formulas are based on a fixed case reference temperature.

Single sequence of m power dissipation pulses

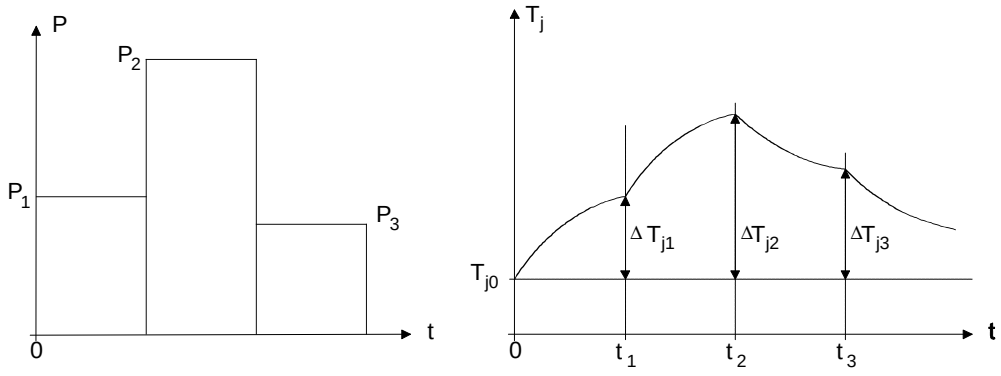


Figure 3.10 Power dissipation and junction temperature at single sequence of m power dissipation pulses versus time

Junction temperature alteration at t_1:

$$\Delta T_{j1} = P_1 \cdot \sum_{\nu=1}^{n} R_{th\nu}\left[1 - \exp\left(-t_1/\tau_{th\nu}\right)\right] \tag{3.13}$$

Junction temperature alteration at t_2:

$$\Delta T_{j2} = P_1 \cdot \sum_{\nu=1}^{n} R_{th\nu}\left[1 - \exp\left(-t_2/\tau_{th\nu}\right)\right] + \left(P_2 - P_1\right) \cdot \sum_{\nu=1}^{n} R_{th\nu}\left[1 - \exp\left(-\left(t_2 - t_1\right)/\tau_{th\nu}\right)\right] \quad (3.14)$$

Junction temperature alteration at t_m:

$$\Delta T_j(t_m) = \sum_{\mu=1}^{m} \left(P_\mu - P_{\mu-1}\right) \cdot \sum_{\nu=1}^{n} R_{th\nu}\left[1 - \exp\left(-\left(t_m - t_{\mu-1}\right)/\tau_{th\nu}\right)\right] \quad (3.15)$$

These formulas are based on a fixed case reference temperature.

3.2.2.3 Junction temperature under pulse operation

The transistor and diode Z_{thjc}-characteristics under periodic pulse conditions indicated in the datasheets may be used for calculation of the average and maximum junction temperature under power dissipation load periodically repeated along with the pulse frequency.
Figure 3.11 shows such a set of curves for the IGBT and the diode of a SKM100GB123D module and a typical current and junction temperature characteristic in the transistor under pulse operation.

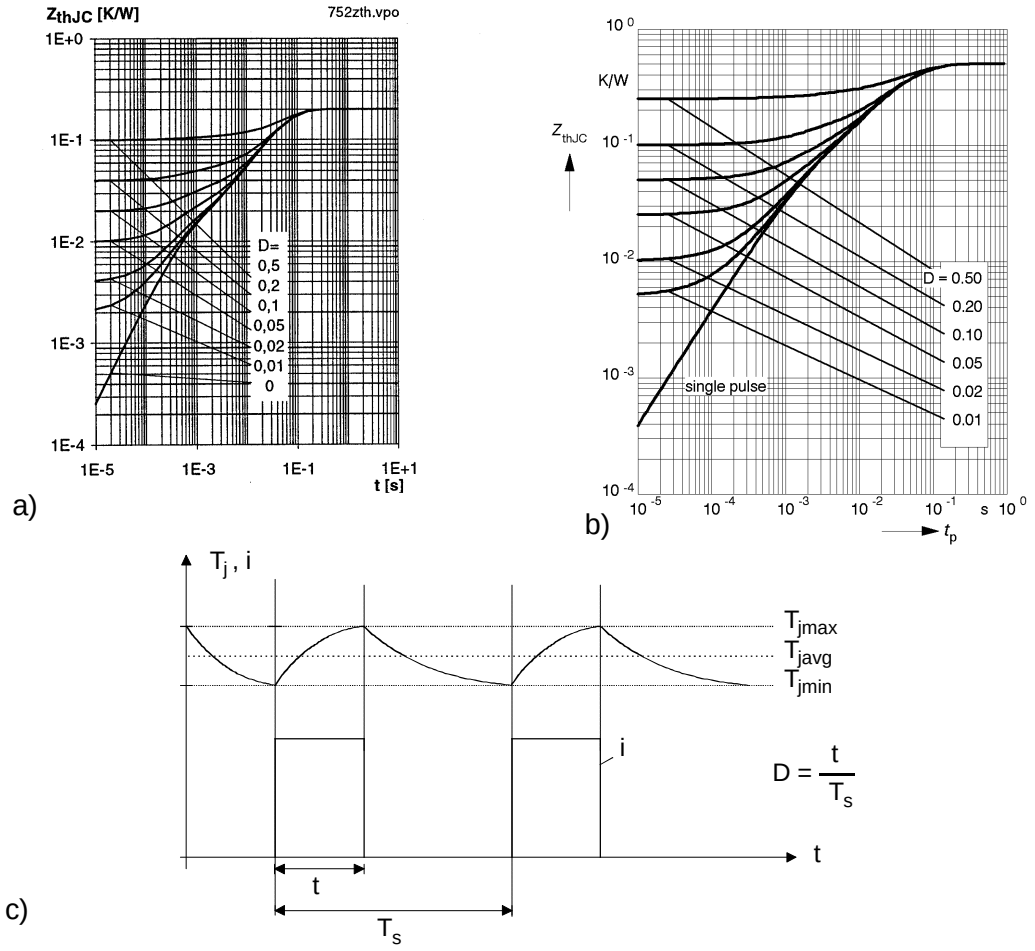


Figure 3.11 Transient thermal impedance Z_{thjc} of IGBT (a) and diode (b) of a SKM100GB123D module
c) Current and temperature characteristic

The average junction temperature T_{javg} results from multiplication of the thermal resistance R_{thjc} with the average power dissipation P_{totavg}. The latter is calculated by averaging the energy dissipation per pulse over the whole pulse or switching duration T_s.

$P_{totavg} = f_s * (E_{on} + E_{off} + E_{fw})$

$T_{javg} = T_c + P_{totavg} * R_{thjc}$

The maximum junction temperature T_{jmax} results from multiplication of Z_{thjc} under pulse operation with the maximum power dissipation P_{totmax}. The latter is calculated by averaging the energy dissipation per pulse over the on-state time t of transistor or diode, respectively, within the pulse duration T_s.

$P_{totmax} = (E_{on} + E_{off} + E_{fw})/t$

$T_{jmax} = T_c + P_{totmax} * Z_{thjc}$

Examples with a SKM100GB123D IGBT:

Example 1: $f_s = 10$ kHz; $T_s = 100$ µs; $D_T = 0.2$; $t = 20$ µs
$T_c = 80°C$; $E_{on} + E_{off} + E_{fw} = 25$ mJ
$R_{thjc} = 0.2°C/W$, $Z_{thjc} = 0.04°C/W$ (see Figure 3.11a)

Consequently: $P_{totavg} = 250$ W; $P_{totmax} = 1250$ W
$T_{javg} = 80°C + 250\ W * 0.2°C/W =$ **130°C**
$T_{jmax} = 80°C + 1250\ W * 0.04°C/W =$ **130°C**

Example 2: $f_s = 2$ kHz; $T_s = 500$ µs; $D_T = 0.2$; $t = 100$ µs
$T_c = 80°C$; $E_{on} + E_{off} + E_{fw} = 25$ mJ
$R_{thjc} = 0.2°C/W$, $Z_{thjc} = 0.042°C/W$ (see Figure 3.11a)

Consequently: $P_{totavg} = 50$ W; $P_{totmax} = 250$ W
$T_{javg} = 80°C + 50\ W * 0.2°C/W =$ **90°C**
$T_{jmax} = 80°C + 250\ W * 0.042\ °C/W =$ **90.5°C**

Example 3: $f_s = 2$ kHz; $T_s = 500$ µs; $D_T = 0.2$; $t = 100$ µs
$T_c = 80°C$; $E_{on} + E_{off} + E_{fw} = 125$ mJ
$R_{thjc} = 0.2°C/W$, $Z_{thjc} = 0.042°C/W$ (see Figure 3.11a)

Consequently: $P_{totavg} = 250$ W; $P_{totmax} = 1250$ W
$T_{javg} = 80°C + 250\ W * 0.2°C/W =$ **130°C**
$T_{jmax} = 80°C + 1250\ W * 0.042°C/W =$ **132.5°C**

Example 4: $f_s = 50$ Hz; $T_s = 20$ ms; $D_T = 0.5$; $t = 10$ ms
$T_c = 80°C$; $E_{on} + E_{off} + E_{fw} = 5$ J
$R_{thjc} = 0.2°C/W$, $Z_{thjc} = 0.12°C/W$ (see Figure 3.11a)

Consequently: $P_{totavg} = 250$ W; $P_{totmax} = 500$ W
$T_{javg} = 80°C + 250\ W * 0.2°C/W =$ **130°C**
$T_{jmax} = 80°C + 500\ W * 0.12°C/W =$ **140°C**

Example 1 is calculated based on a typical IGBT pulse frequency of 10 kHz. The result shows that there is no deviation between the average and maximum values of the junction temperature due to the low thermal impedances at high frequencies.
The pulse frequency in example 2 and 3 had been reduced to 2 kHz, however keeping constant values for the amount of energy dissipation in example 2 and for the average and maximum total power dissipation in example 3. Both examples show a deviation between average and maximum junction temperature.
Simply expressed, it may be presumed that a calculation based on average power dissipation and static thermal resistance is sufficient for pulse frequencies above about 3 kHz.
Example 4 shows the drastic difference between average and maximum junction temperature at very low pulse frequencies.

3.2.2.4 Junction temperature at fundamental harmonics frequency

Calculation of the junction temperature determined by the fundamental frequency of the converter output current is only efficient, when it is computer-aided.
The thermal system as well as the electrical system per pulse duration have to be calculated in detail in order to integrate the IGBT and diode junction temperature over a sine half-wave.
Figure 3.12 shows a principal calculation scheme which had been elaborated in source [194].

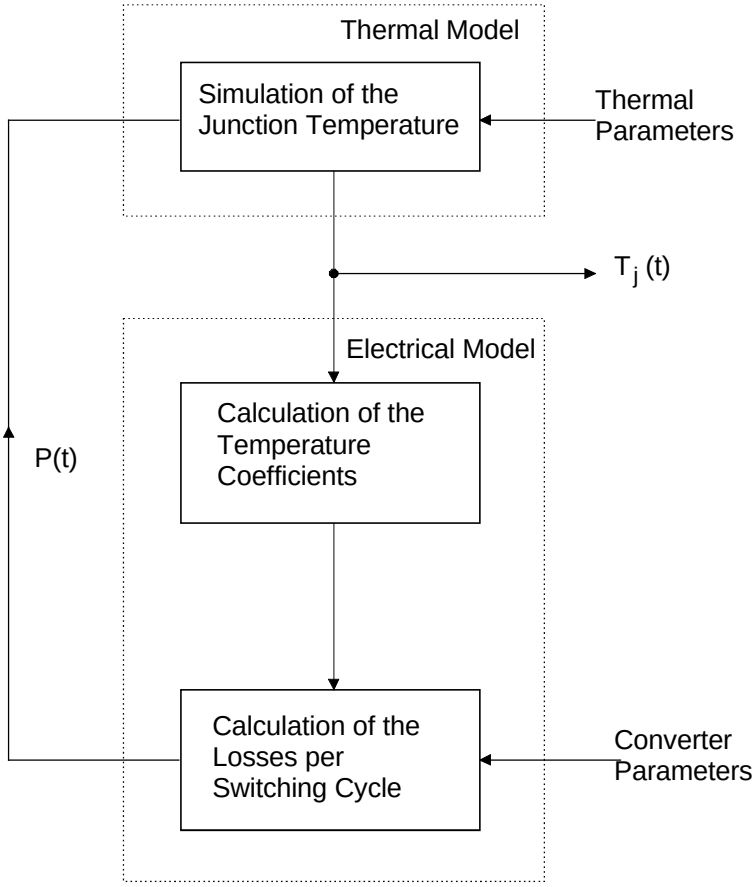


Figure 3.12 Principal calculation of the junction temperature in converters with sinusoidal output currents [194]

The thermal model mainly corresponds to Figure 3.8 simulating the thermal impedances by means of RC-elements.
Switching losses per pulse may be calculated based on stored characteristics, if the current converter parameters such as DC-link voltage and instantaneous load current are given. The

instantaneous junction temperature is entered into the calculation via the temperature coefficients.

Figure 3.13 shows the power dissipation time characteristic and the average power dissipation in an IGBT as well as the resulting junction temperature characteristics for different basic output frequencies as the result of a simulation according to [194].

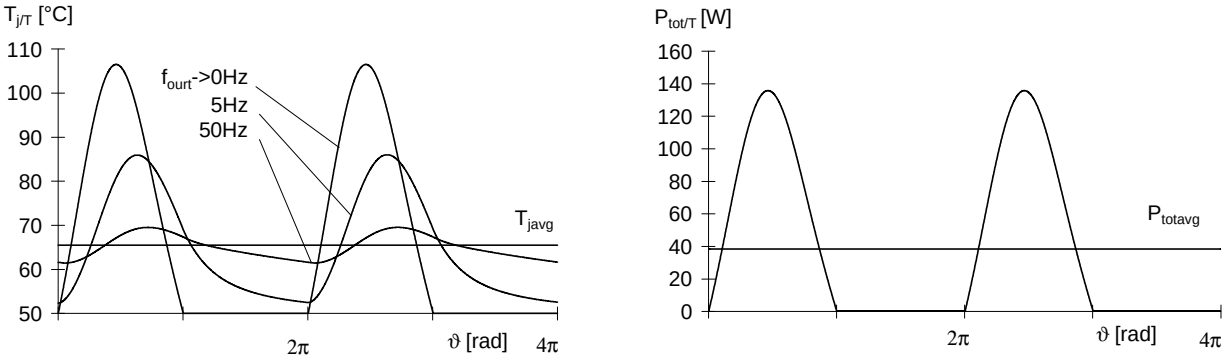
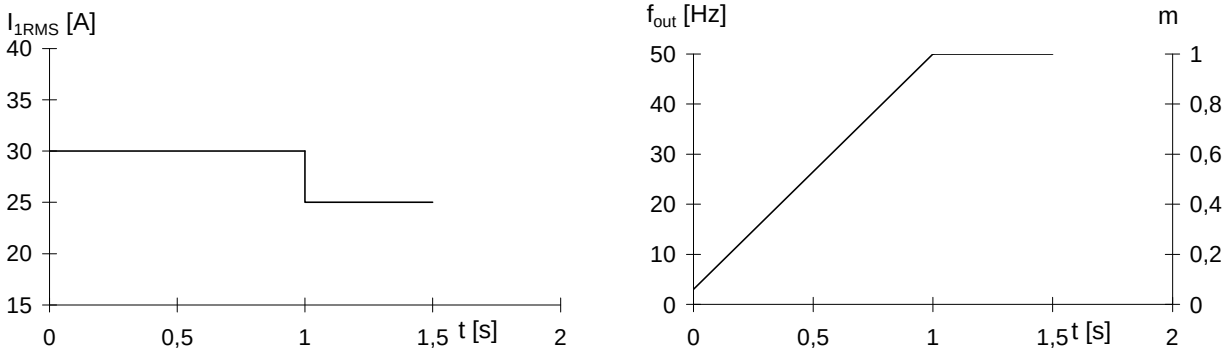


Figure 3.13 Simulated junction temperature and power dissipation characteristics of a 1200V/50A-IGBT under inverter operation for different fundamental output frequencies; [194]
v_d = 540 V; i_{1RMS} = 25 A, f_s = 8 kHz; cos φ = 0.8; m = 0.8; T_h = 50°C

In this example, the maximum junction temperature exceeds the average value by just about 4-5 K at a frequency of 50 Hz.
For low frequencies the average junction temperature is no longer permitted to determine the thermal layout of the system because of its clearly increased maximum value.
Consequently, the permissible output current RMS-Valuefor a defined power module will decrease at a given heatsink temperature and switching frequency.
Corresponding performance characteristics (e.g. for SKiiPPACK) are available by SEMIKRON on request.
Moreover, Figure 3.13 shows that no temperature ripples with righ pulse frequency arise. This is also confirmed by the calculations in chapter 3.2.2.3.

A very particular special case with regards to the thermal stress of power modules is the voltage- and frequency-controlled starting procedure of a three-phase motor drive supplied by an inverter. Figure 3.14 shows a related simulation example.



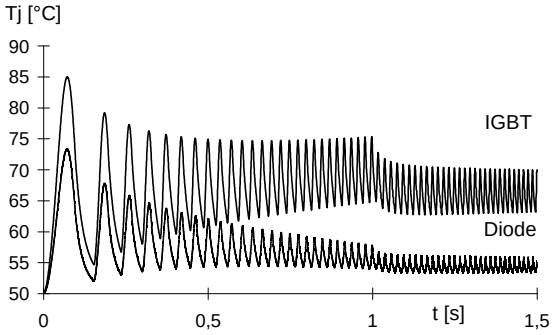


Figure 3.14 Start-up of a three-phase motor drive (parameters as in Figure 3.13), [194]

3.2.3 Evaluation of temperature characteristics with regards to module life

Power dissipation alterations below a repetition frequency of about 3 kHz will not be smoothed by the transient thermal impedance of the chips any longer and will lead to temperature fluctuations in the module (see chapter 3.2.2).
As already mentioned in chapter 1.4.2.4, all internal connections of power modules are subject to wear and tear caused by temperature fluctuations. This fatigue of material is caused by thermal stress due to the different expansion coefficients of the connected materials.

Therefore, it is important for thermal dimensioning to check, whether the chip temperature fluctuations generated during periodic power cycling (pulse frequency, fundamental frequency, power cycle) are so intensive that, in the worst case, the required number of cycles may not be reached. In this case, not the maximum chip temperature T_{jmax}, but the temperature difference $\Delta T_j = T_{jmax} - T_{jmin}$ during given power cycles is considered as limit value for power losses of the module.

The correlation between the possible number of power cycles n and the temperature cycling amplitude ΔT_j is subject to the influence of many parameters. Corresponding measurements require a lot of time and effort, see chapter 2.7 and [231].

In tests with active power cycles the lifetime of a power module depends not only on the temperature difference ΔT_j but also on the average (medium) temperature T_m in the test procedure. This was confirmed clearly by the results of LESIT-research project [303].
LESIT results of power cycling lifetime tests with power modules by different manufacturers are shown in Figure 3.15. The parameter adjustment was done by SEMIKRON. These results represent the state-of-the-art in 1995. Meanwhile, the lifetime was increased by improved solder connections and optimized wire bond connections. So, 20000 cycles at ΔT=100°C and $T_{j,min}$=40°C are achieved. Presently, updated characteristics for SEMIKRON power modules are in preparation.

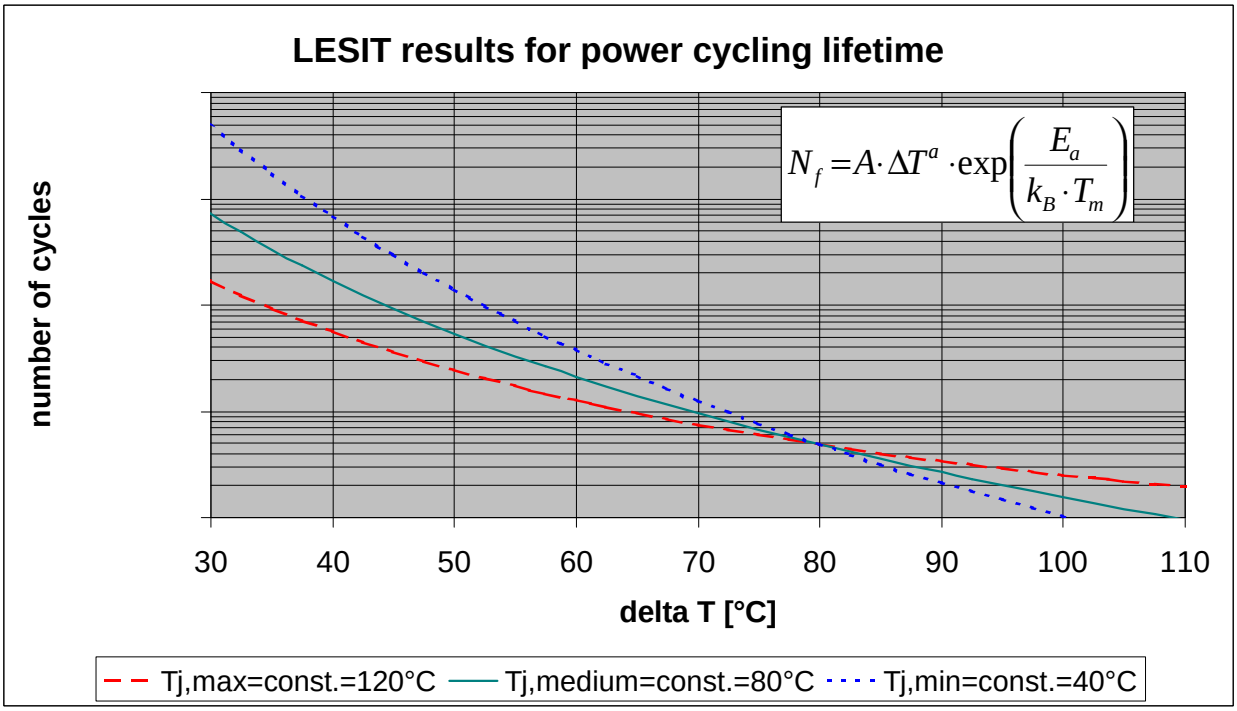


Figure 3.15 LESIT results for power cycling lifetime

3.3 Cooling of power modules

3.3.1 Cooling devices, coolants and cooling methods

The heat potential due to forward, switching and blocking losses in power modules has to be dissipated by means of heatsinks, which provide an expanded surface for convection and radiation, spreading the heat flow as well as reducing the intensity of transient thermal processes. Due to their isolation, all power modules of one system are mounted on to one common heatsink which may also serve as an element of the construction (case, chassis etc.).

Heat dissipation in a heatsink works on the principle that the heat is dissipated to the coolant either by direct heat transmission or via a heat carrier.
Heat carriers may be air, water or (more rarely) isolation oil, which is circulated by the effect of gravity or by fans or pumps.
Air in natural and forced motion or coolant mixtures on the basis of water may serve as coolants.
In the following we would like to emphasise only natural (free convection) and forced air cooling and water cooling systems with one coolant circuit each, since more sophisticated cooling methods, such as “heatpipes” or boiling cooling are normally extremely application-specific and oil cooling is not very commonly used with power modules.

The heatsink material has to be constructed for optimal heat spreading (high heat transfer coefficient λ), with acceptable material and handling costs. Therefore, aluminum is often preferred (λ = 247 W/K*m for pure Al), in special cases copper is also used (λ = 398 W/K*m).
The dependence of heat spreading on the production process and the alloy used is remarkable; practical heatsinks show λ-values between 150 W/K*m (Al-die cast alloy) and 220 W/K*m (AlMgSi-extruded material).

Heat spreading has a considerable influence on the thermal efficiency of the heatsink. Therefore, optimized dimensioning of root thickness, number of fins, fin height and fin thickness is of importance:

- The *root* of a heatsink is the unfinned part of the mounting surface for the power modules, where the temperature gradient to the module base plate is relatively low and where the heat is spread.
- The *fins* of an air heatsink are used for dissipating the majority of the heat to the environment by radiation and convection. In water heatsinks this task is fulfilled by more or less structured *water channels*.

  $R_{thha} = \Delta T/P_{tot} = 1/(\alpha * A)$

  results from $Q = \alpha * A * \Delta T = P_{tot}$

  (Q: dissipated heat quantity, α: heat transfer coefficient, A: heat transfer area, ΔT: temperature difference to the environment, P_{tot}: power dissipation, R_{thha}: heat transfer resistance of the heatsink)

  It is recommended that a high number of fins is provided in order to increase the area of dissipation. But it has to be guaranteed that the flow conditions are set in a way which will not decrease α greatly.

Consequent to this conclusion, the different optimization criteria for heatsinks with natural and forced air cooling may be deducted.

The heatsink is heated more evenly when the power dissipation increases, i.e. the efficient heat exchange surfaces are enlarged; in Figure 3.16 the heat exchange surface is further extended by an increased heatsink length.

3.3.2 Thermal model of the cooling device

When explaining the thermal characteristics of power modules in chapter 1.4.2.2, the heatsink in the thermal equivalent block diagram had been described by only one “RC-element” (R_{thha}, Z_{thha}).
However, with an increase of power dissipation at t = 0 from P = 0 to P = P_m , the characteristic of the transient thermal impedance of the heatsink Z_{thha}versus time t is split up into several time constants as shown in Figure 3.16 with an example. The total thermal impedance characteristic Z_{thja}(t) of the assembly may be determined by graphic addition of the thermal impedance characteristics of the power module and the heat transition to the heatsink.
The Z_{th}(t)-curves may be plotted as the sum of ν exponential functions using the following equations:

$$\Delta T(t) = P_m \cdot \sum_{\nu} R_{th\nu}\left[1 - \exp\left(-t/\tau_{th\nu}\right)\right] \qquad \text{and} \qquad Z_{thha}(t) = \Delta T(t)/P_m$$

i.e.

$$Z_{thha}(t) = \sum R_{thv}\left[1 - \exp\left(-t/\tau_{thv}\right)\right]$$

The number of ν and the $R_{thν}$- and $\tau_ν$-values are chosen so that a sufficient approximation of the characteristic can be produced without applying complicated calculation procedures, independent of the physical structure. One iteration method is described, for example, in source [266].
The ratings for simulations indicated by SEMIKRON and mentioned briefly in the following chapters are based on a 4-time-constants-model (ν = 4).

3.3.3 Natural air cooling (free convection)

Natural air cooling is applied in low power range applications up to 50 W as well as in high power range applications, if the use of fans is not possible or if extremely large cooling surfaces are available in the device.
Since with free convection, the thermal transient resistance of the heatsinks usually exceeds the internal thermal resistance of the power modules, the temperature difference between chip (125°C) and cooling air (45°C) drops mainly over the heatsink. Near the modules, the heatsink temperature is usually higher than with forced air cooling, for example 90...100°C. Because power losses are usually low with natural air cooling, heatsink root and fins do not have to be very thick, since heat conductivity has only a minor influence on the thermal features. The fin distances have to be selected sufficiently to obtain a favourable ratio between air uplift (drop of temperature / density) and air friction. Black coating of the heatsink will improve the radiation characteristics and, thus, the R_{thha}-value by about 15 % at a temperature difference of 50 K between mounting surface and atmosphere [266]. The surface finish, however, does not impair heat transfer between module base plate and heatsink.

3.3.4 Forced air cooling

In contrast to natural air cooling, forced air cooling can reduce the thermal heatsink resistance to 1/5...1/15. Figure 3.16 compares the $Z_{thha}(t)$ characteristics of natural and forced air cooling up to the final R_{thha}-value with the example of different SEMIKRON P16/...-heatsinks.

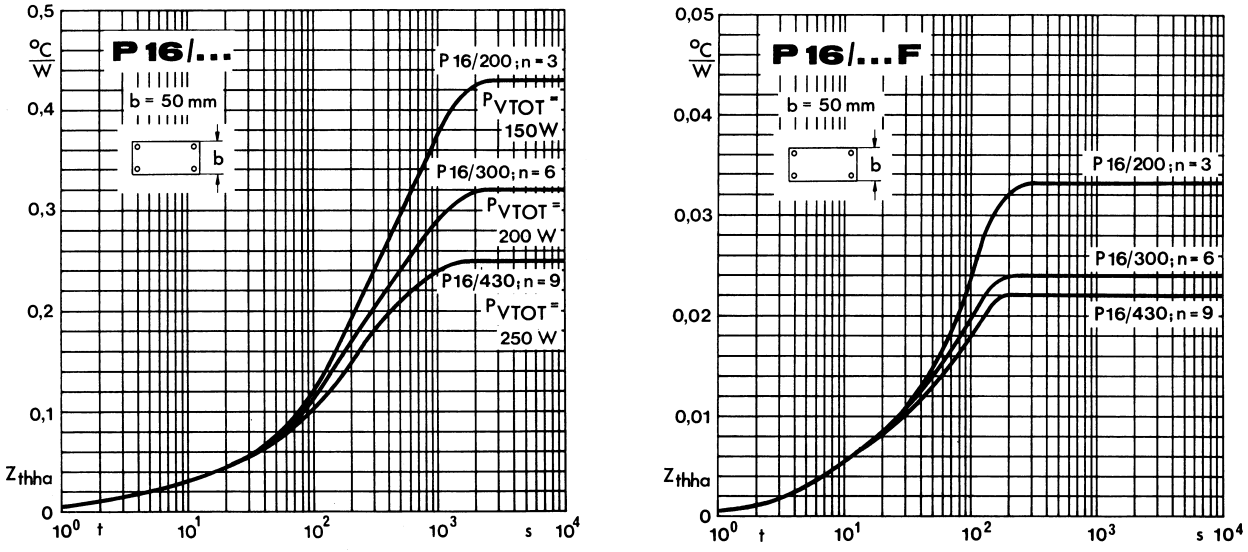


Figure 3.16 $Z_{thha}(t)$-characteristics for different P16/...-heatsinks
a) Free convection
b) Forced air cooling

Compared to free convection, α is much higher with forced air cooling. The rated surface temperature of forced air-cooled heatsinks should not exceed 80...90°C at a supply air temperature of 35°C (condition for datasheet ratings).

The heat conductivity of the heatsink has tremendous influence on the cooling effect, which requires a thick root and a maximum number of fins. Because convection is mainly responsible for the dissipation of heat, black coating of the heatsink will have almost no effects with forced air cooling.

R_{thha} is mainly determined by the rate of air flow per time V_{air}/t, depending on the average cooling air velocity v_{air} and the transfer cross section A:

$V_{air}/t = v_{air} * A$

Instead of the assumed laminar air flow, air whirlings on the fin surfaces will effect turbulent flow conditions between the fins, which will improve heat dissipation to the atmosphere, provided the fin surfaces are set out accordingly.
The transfer cross section of the heatsink will be reduced by increased number of fins and fin width as well as by increased heatsink length (fin length L) and the cooling air-pressure drop Δp will rise. Consequently, heat dissipation is dependent on the characteristics of the fan, which are described in the fan characteristic $\Delta p = f(V_{air}/t)$ (Figure 3.17).

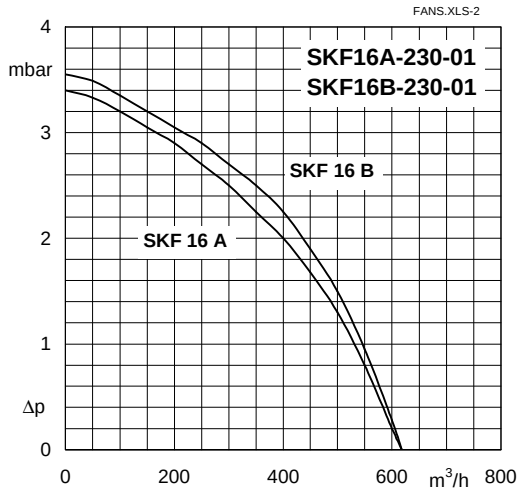


Figure 3.17 Fan characteristic $\Delta p = f(V_{air}/t)$ for SEMIKRON P16/... fans

The thermal transient resistance of the heatsink assembly R_{thha} depends on the rate of air flow shown in Figure 3.19, which may be determined by combining fan and pressure drop characteristics $\Delta p = f(V_{air}/t, L)$ or $\Delta p = f(v_{air}, L)$ of the heatsink.

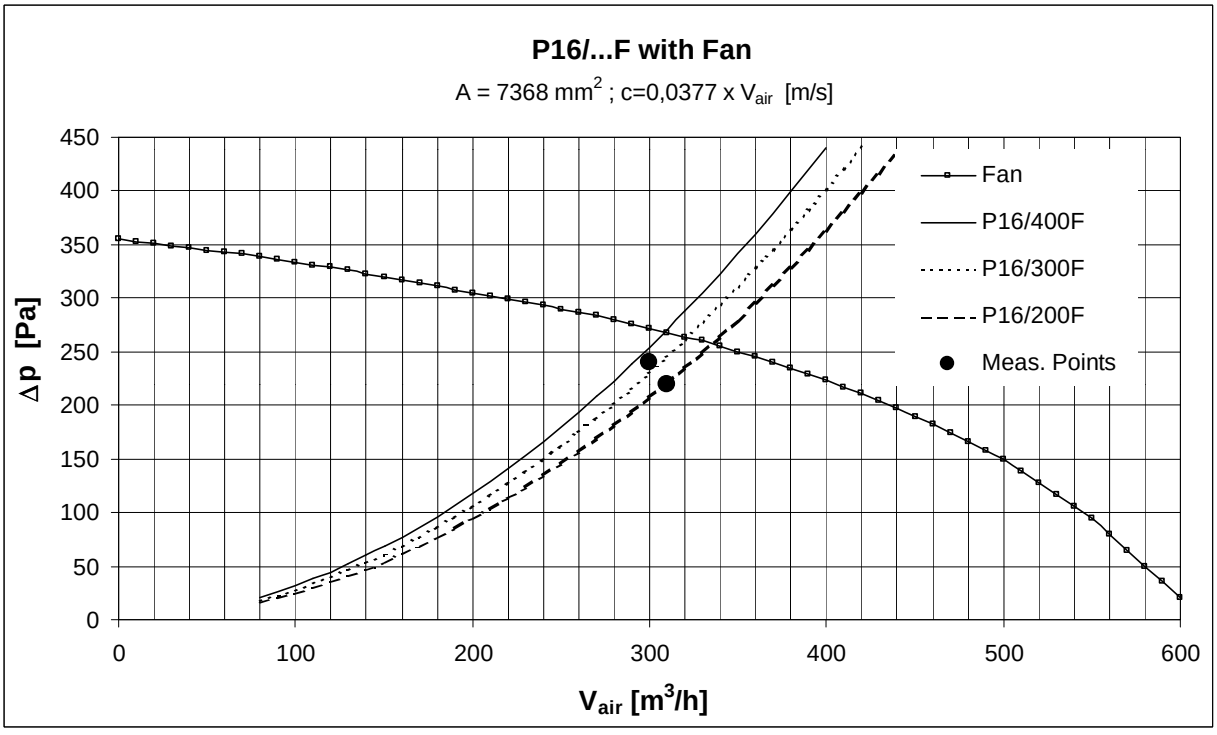


Figure 3.18 Air flow of a P16/... heatsink profile at various heatsink length

Apart from the air flow, R_{thha} is dependent on distribution and position of heat sources (power modules) on the heatsink. Figure 3.19 explains these relationships with the example of a selected SKiiP-assembly.

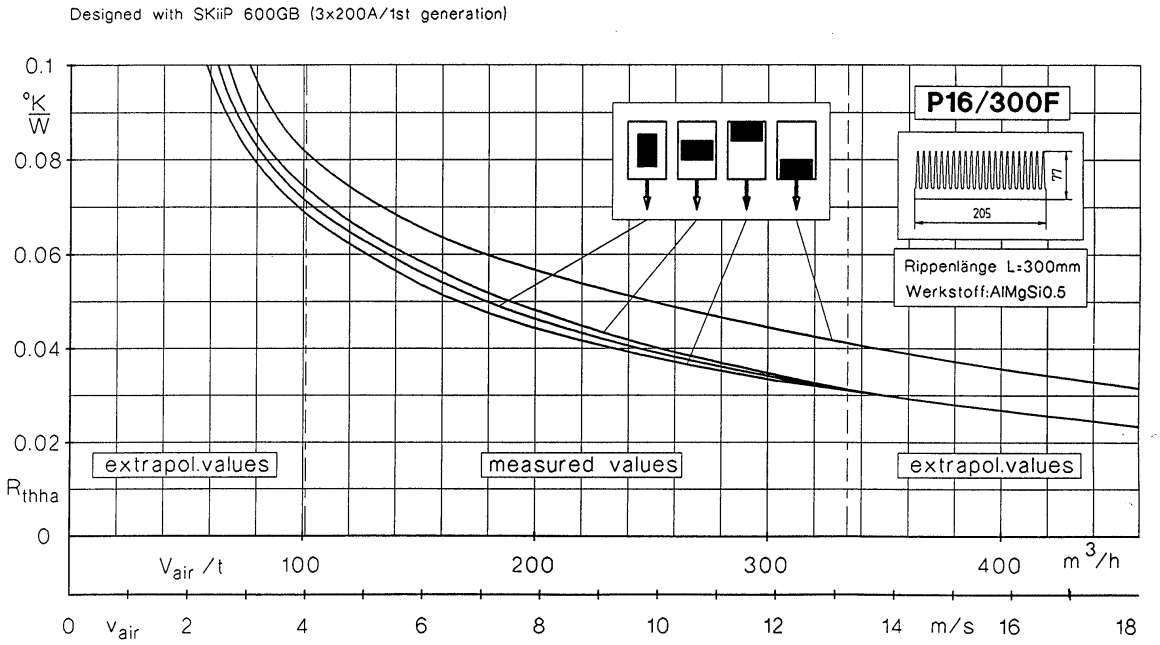


Figure 3.19 Thermal resistance of the heatsink R_{thha} of a SKiiP-assembly versus air flow and position of the SKiiPPACK on the heatsink

Figure 3.20 shows the standard assembly of a 3-fold SKiiPPACK on an air-cooled heatsink P16/280F.

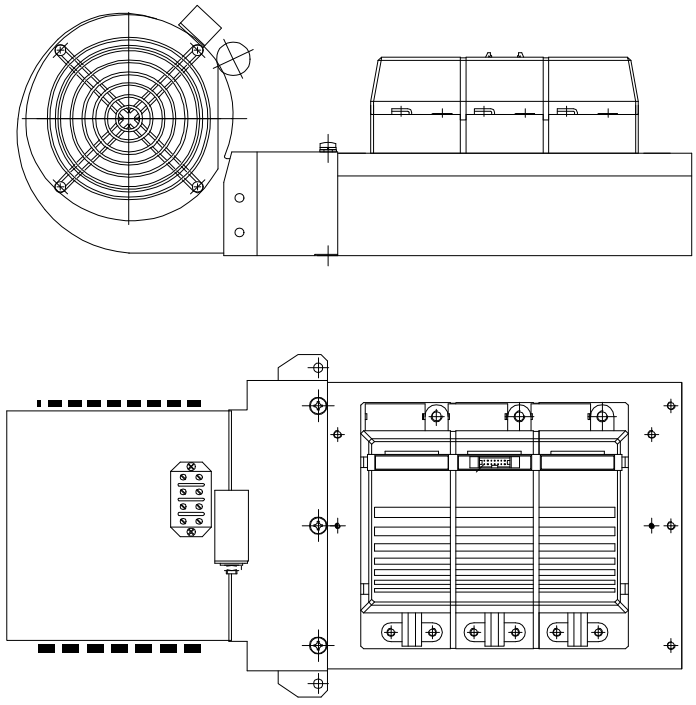


Figure 3.20 SKiiPPACK 3 standard assembly with SKF 16B fan

To determine optimized conditions for forced air cooled heatsink profiles, heat conduction and convection can also be integrated by the fin height layout, which will result in the following formula on condition of some simplifications:

$$R_{thha} = \frac{1}{n \cdot \sqrt{a \cdot U \cdot l \cdot A} \cdot \left[\frac{1}{1 + \exp - 2kh} - \frac{1}{1 + \exp 2kh} \right]}$$

with $k = \sqrt{\frac{a \cdot U}{l \cdot A}}$

(α: heat-transfer coefficient, U: fin circumference, λ: coefficient of thermal conductivity of heatsink, A: cross section of fins, h: fin height)

Often, several heatsinks have to be cooled by only one fan, for which they are either arranged in parallel (heatsinks positioned side by side) or in series (heatsinks behind each other in direction of air flow).
With regard to thermal stacking, which is preferred, for example, in three-phase inverter applications with standard GB-circuit SKiiPPACKs (halfbridge modules), special attention should be paid to the fact that the air is preheated for 2 of the 3 SKiiPPACKs, which has to be taken into consideration when determining the thermal layout.
At an air flow rate of 300 m^3/h, about 10 K temperature difference between supply and exhaust air is presupposed as a standard value per kW dissipated power. Thermal details are given in chapter 3.3.6.1.

3.3.5 Water cooling

Water cooling of power modules can be used for special high power inverters (MW-range) as well as for small power devices, which already provide for a water circuit due to their working principles (e.g. car drives, galvanic plants, inductive heating).
Mostly, the admission temperature of the coolant values is up to 50..70°C when the heat of the coolant is directly dissipated to the atmosphere; in industrial plants with active heat exchangers the temperature is about 15..25°C.

The temperature difference between heatsink surface and coolant which is lower than with air cooling may be utilized in two ways:
- increased energy exchange at a high dynamic ΔT_j of chip temperature per cycle (limits for module life see chapter 3.2.3) or
- low chip temperature, long module life.

Due to its capability for high heat retention (thermal capacity c_p = 4.187 kJ/kg $*$K) water is principally preferred to oil or glycol for the dissipation of heat.

Figure 3.21 shows a SEMIKRON standard assembly with a 3-fold SKiiPPACK on a water-cooled base plate.

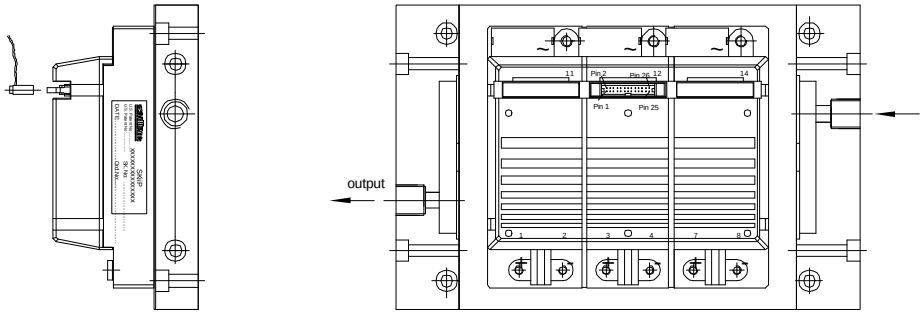


Figure 3.21 SKiiPPACK 3 standard assembly with water-cooled base plate

Due to the corrosive effect of water and the mostly required frost-resistance, open or closed circuit with pure water are hardly used.
By adding glycol, for example, the heat-retainability of the coolant will be diminished (e.g. 3.4 kJ/(kg∗K) at an addition of 50 % glycol and a coolant temperature of 40°C). As viscosity and specific gravity of the coolant will rise, the thermal resistance from heatsink to coolant R_{thhw} will considerably increase together with the share of glycol. Compared to pure water, a 50 % addition of glycol will effect an increase of R_{thhw} by approximately 50...60 % and again by another 60...70 %, if the glycol share is increased up to 90 %.
To guarantee for corrosion protection, SEMIKRON water-cooled aluminum heatsinks contain a minimum share of glycol of 10 %. The hardness of the cooling water may not exceed a degree of 6. At least for coolant temperatures higher than 60°C we recommend to use a closed cooling circuit.

Thermal stacking of heatsinks with power modules or SKiiPPACKs is also done in correlation with water cooling. A difference of about 1.7 K per kW dissipated power between inlet and outlet temperature of the coolant can be taken as a standard value for the preheating per heatsink (SEMIKRON water-cooled heatsinks for SKiiPPACKs) for a 50/50 % water-glycol-mixture at a coolant flow of 10 l/min.
For detailed information on SKiiPPACKs on water-cooled heatsinks please see chapter 3.3.6.2.

3.3.6 Heatsink ratings for SKiiPPACKs on standard heatsinks

3.3.6.1 Forced air cooling

The following table contains the characteristics R_ν and τ_ν for thermal calculation according to the 4-time-constants-model for SKiiPPACKs on standard heatsink P16 with fan SKF 16B (GD 133-2k-40105).

$R_{thsa\ tot}$: stationary thermal resistance as a result of the temperature difference between temperature sensor (T_s) and supply air (T_a), with reference to the total power dissipation P_{tot} of the assembly

$$R_{thsa\ tot} = \sum_{\nu=1}^{4} R_\nu$$

$Z_{thsa\ tot}$: transient thermal impedance as a result of the temperature difference between temperature sensor (T_s) and supply air (T_a),with reference to the total power dissipation P_{tot} of the assembly

$$Z_{thsa\ tot} = \sum_{\nu=1}^{4} R_\nu \cdot \left[1 - \exp\left(-t/\tau_\nu\right)\right]$$

thermal characteristics (4-constants-model)									
	R_1 K/W	R_2 K/W	R_3 K/W	R_4 K/W	ΣR K/W	τ_1 s	τ_2 s	τ_3 s	τ_4 s
2-fold SKiiPPACK (V_{air}/t = 310 m^3/h)									
	$1.383 \cdot 10^{-2}$	$1.886 \cdot 10^{-2}$	$6.663 \cdot 10^{-3}$	$3.640 \cdot 10^{-3}$	$4.299 \cdot 10^{-2}$	$2.579 \cdot 10^{2}$	$6.350 \cdot 10^{1}$	5.831	$1.543 \cdot 10^{2}$
3-fold SKiiPPACK (V_{air}/t = 305m^3/h)									
	$1.157 \cdot 10^{-2}$	$1.669 \cdot 10^{-2}$	$3.512 \cdot 10^{-3}$	$3.097 \cdot 10^{-3}$	$3.487 \cdot 10^{-2}$	$2.638 \cdot 10^{2}$	$6.625 \cdot 10^{1}$	6.049	$2.000 \cdot 10^{-2}$
4-fold SKiiPPACK (V_{air}/t = 300m^3/h)									
	$1.398 \cdot 10^{-3}$	$2.048 \cdot 10^{-2}$	$7.012 \cdot 10^{-3}$	$2.448 \cdot 10^{-3}$	$3.134 \cdot 10^{-2}$	$5.398 \cdot 10^{2}$	$1.724 \cdot 10^{2}$	$2.008 \cdot 10^{1}$	$2.876 \cdot 10^{-2}$

In the case of thermal stacking of SKiiPPACKs, the reduction of air flow resulting from the increased pressure drop and pre-heating of the “backward” SKiiPACKs by the cooling air passing the “front” SKiiPPACKs has to be considered in the calculations.
Figure 3.22 explains the principle of thermal stacking:

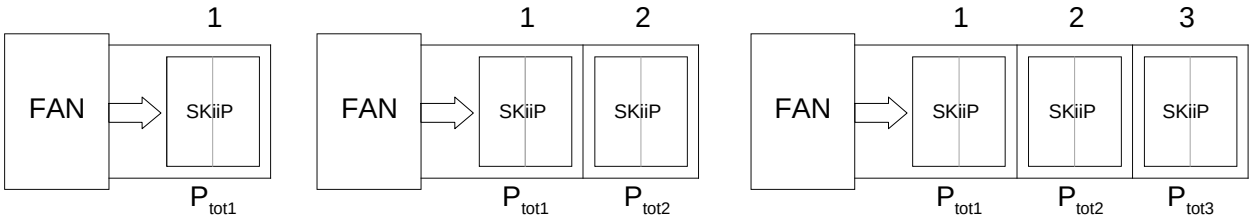


Figure 3.22 Thermal stacking of SKiiPPACKs with forced air cooling

Pre-heating is determined by total power dissipation of the SKiiPPACKs P_{totn}, stationary thermal resistance R_{thaa} and transient thermal impedance Z_{thaa} (resistance R_{thaa}/time constant τ_{aa}) between two adjacent heatsinks, see Figure 3.22. The following formulas are valid for determining the transient thermal impedances $Z_{thsatotn}$ of every single SKiiPPACK:

SKiiPPACK no. 1

$$Z_{thsa\ tot1} = \sum_{\nu=1}^{4} R_\nu \cdot \left[1 - \exp\left(-t/\tau_\nu\right)\right]$$

SKiiPPACK no. 2

$$Z_{thsa\ tot2} = \sum_{\nu=1}^{4} R_\nu \cdot \left[1 - \exp\left(-t/\tau_\nu\right)\right] + \left(P_{tot1}/P_{tot2}\right) \cdot R_{thaa1-2} \cdot \left[1 - \exp\left(-t/\tau_{aa1-2}\right)\right]$$

SKiiPPACK no. 3

$$Z_{thsa\ tot3} = \sum_{\nu=1}^{4} R_\nu \cdot [1 - \exp(-t/\tau_\nu)] + [(P_{tot1} + P_{tot2})/P_{tot3}] \cdot R_{thaa2\text{-}3} \cdot [1 - \exp(-t/\tau_{aa\,2-3})]$$

3.3.6.2 Liquid cooling

The following table contains the characteristics R_ν and τ_ν for thermal calculation according to the 4-time-constants-model for SKiiPPACKs on a standard water-cooled heatsink S1021450 with mutual water inlet/outlet, 50/50 % water-glycol-mixture at a coolant temperature of 50°C. Since the temperature T_s of the internal temperature sensor of the SKiiP is also available here as a reference point for the heatsink temperature T_h, the following definitions are valid:

$R_{thsw\ tot}$: stationary thermal resistance as a result of the temperature difference between temperature sensor (T_s) and coolant (T_w), with reference to the total power dissipation P_{tot} of the assembly.

$$R_{thsw\ tot} = \sum_{\nu=1}^{4} R_\nu$$

$Z_{thsw\ tot}$: transient thermal impedance as a result of the temperature difference between temperature sensor (T_s) and coolant (T_w),with reference to the total power dissipation P_{tot} of the assembly.

$$Z_{thsw\ tot} = \sum_{\nu=1}^{4} R_\nu \cdot [1 - \exp(-t/\tau_\nu)]$$

Coolant by-pass l/min	thermal characteristics (4-constants-model)								
	R_1 K/W	R_2 K/W	R_3 K/W	R_4 K/W	ΣR K/W	τ_1 s	τ_2 s	τ_3 s	τ_4 s
2-fold SKiiPPACK									
6	$1.942 \cdot 10^{-3}$	$6.262 \cdot 10^{-3}$	$3.785 \cdot 10^{-3}$	$6.608 \cdot 10^{-3}$	$1.860 \cdot 10^{-2}$	$1.225 \cdot 10^{-1}$	2.911	$1.189 \cdot 10^{1}$	$5.196 \cdot 10^{1}$
10	$1.942 \cdot 10^{-3}$	$6.262 \cdot 10^{-3}$	$4.402 \cdot 10^{-3}$	$2.993 \cdot 10^{-3}$	$1.560 \cdot 10^{-2}$	$1.225 \cdot 10^{-1}$	2.911	$1.782 \cdot 10^{1}$	$1.131 \cdot 10^{2}$
14	$1.942 \cdot 10^{-3}$	$6.262 \cdot 10^{-3}$	$4.628 \cdot 10^{-3}$	$1.667 \cdot 10^{-3}$	$1.450 \cdot 10^{-2}$	$1.225 \cdot 10^{-1}$	2.911	$2.000 \cdot 10^{1}$	$1.355 \cdot 10^{2}$
3-fold SKiiPPACK									
6	$2.143 \cdot 10^{-3}$	$3.818 \cdot 10^{-3}$	$9.405 \cdot 10^{-3}$	$2.535 \cdot 10^{-3}$	$1.790 \cdot 10^{-2}$	$2.204 \cdot 10^{-1}$	3.343	$2.800 \cdot 10^{1}$	$1.123 \cdot 10^{2}$
10	$2.143 \cdot 10^{-3}$	$3.818 \cdot 10^{-3}$	$6.683 \cdot 10^{-3}$	$2.057 \cdot 10^{-3}$	$1.470 \cdot 10^{-2}$	$2.204 \cdot 10^{-1}$	3.343	$2.367 \cdot 10^{1}$	$1.094 \cdot 10^{2}$
14	$2.143 \cdot 10^{-3}$	$3.818 \cdot 10^{-3}$	$5.662 \cdot 10^{-3}$	$1.878 \cdot 10^{-3}$	$1.350 \cdot 10^{-2}$	$2.204 \cdot 10^{-1}$	3.343	$2.205 \cdot 10^{1}$	$1.083 \cdot 10^{2}$

4-fold SKiiPPACK									
6	$8.714 \cdot 10^{-4}$	$2.893 \cdot 10^{-3}$	$7.573 \cdot 10^{-3}$	$1.970 \cdot 10^{-3}$	$1.331 \cdot 10^{-2}$	$9.939 \cdot 10^{-2}$	2.038	$2.700 \cdot 10^{1}$	$1.462 \cdot 10^{2}$
10	$8.714 \cdot 10^{-4}$	$2.893 \cdot 10^{-3}$	$4.785 \cdot 10^{-3}$	$2.052 \cdot 10^{-3}$	$1.060 \cdot 10^{-2}$	$9.939 \cdot 10^{-2}$	2.038	$1.868 \cdot 10^{1}$	$9.085 \cdot 10^{1}$
14	$8.714 \cdot 10^{-4}$	$2.893 \cdot 10^{-3}$	$3.649 \cdot 10^{-3}$	$2.086 \cdot 10^{-3}$	$9.499 \cdot 10^{-3}$	$9.939 \cdot 10^{-2}$	2.038	$1.529 \cdot 10^{1}$	$6.830 \cdot 10^{1}$

Calculation of thermal stacking is basically made the same way as with air cooling.

3.4 Power design

MOSFET, IGBT or SKiiP power circuits are designed in printed circuit board technology, or by means of cables or massive copper or aluminum bars, depending on the currents and voltages to be switched.
Apart from the general specifications to be met, for example with regards to creepage and striking distances or current density, the short switching times within the nano to microsecond range demand a sophisticated power design, which also lives up to the requirements of high-frequencies.

3.4.1 Parasitic inductances and capacitances

To analyse the effects of parasitic inductances and capacitances of converters, it will be sufficient to examine one commutation circuit.

Figure 3.23 shows the commutation circuit of an IGBT-inverter with parasitic elements, consisting of DC-link voltage v_d (corresponds to commutation voltage v_K) and two IGBT switches with driver and inverse diodes. Commutation voltage is impressed by the DC-link capacitance C_d. The impressed current i_L flows out of the commutation circuit.

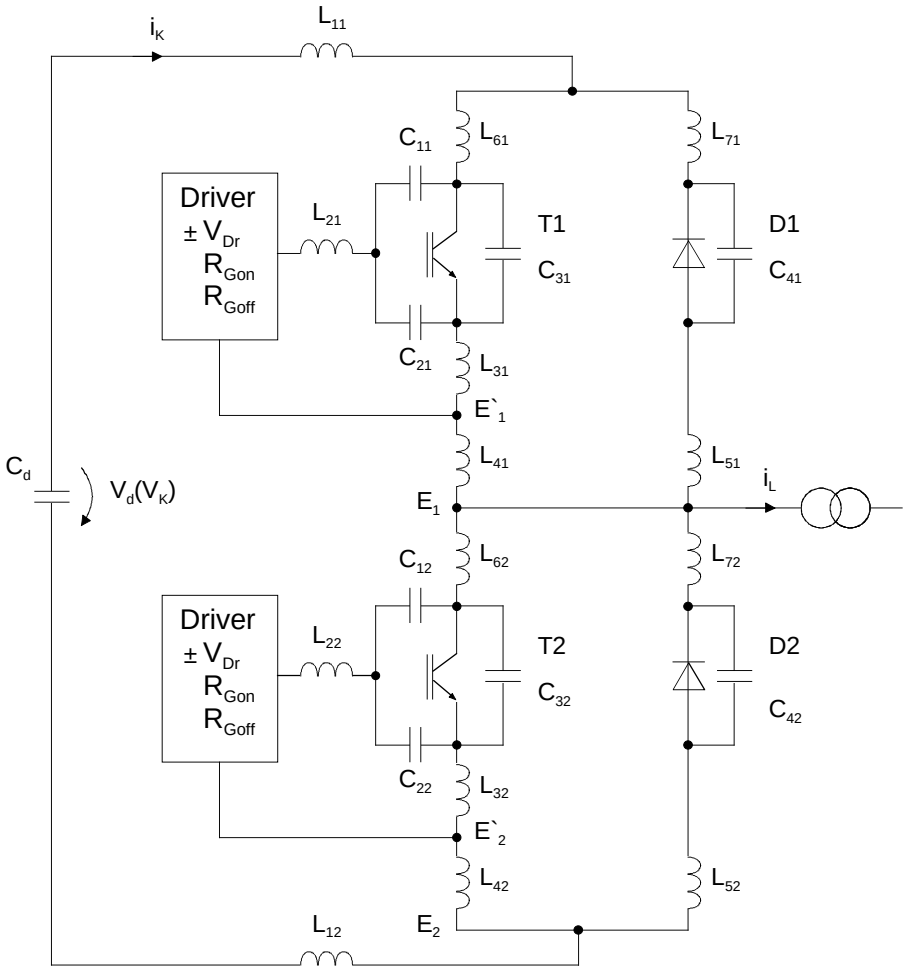


Figure 3.23 Commutation circuit with parasitic elements

The effects of parasitic elements / counter-measures

Total commutation inductance

In the commutation circuit with T1 and D2, the amount of L_{11}, L_{61}, L_{31}, L_{41}, L_{72}, L_{52} and L_{12} is effective as total commutation inductance. In analogy, the amount of L_{11}, L_{71}, L_{51}, L_{62}, L_{32}, L_{42} and L_{12} is effective in the commutation circuit with D1 and T2.

During active turn-on of T1 or T2, respectively, the total commutation inductance becomes effective as turn-on relief, which will reduce turn-on power dissipation in T1 or T2 (see chapter 3.8).

However, during active turn-off of T1 and T2 as well as during reverse-recovery-di/dt of D1 and D2, switching overvoltages are generated in the transistors and diodes due to high di/dt caused by the commutation inductances. This will increase turn-off power dissipation and voltage stress of the power semiconductors.

This effect is especially critical with regards to short-circuits and overload (see chapter 3.6). Moreover, together with parasitic capacitances unwelcome high frequency oscillations may be generated.

Therefore, it is of major importance to minimize inductances in the commutation circuit of hard-switching converters. Except for L_{11} and L_{12}, all inductances are generated in the modules, which may not be influenced by the user. In this respect, it is up to the manufacturers of power

modules, to keep on working on the minimization of internal inductances by improving module assembly technologies (see chapter 1.4).
SEMIKRON datasheets indicate the internal inductances becoming effective at the module output terminals (Example: SKM100GB123D: L_{CE} = max. 30 nH).
In the case of single switch modules (1 IGBT/MOSFET + 1 inverse diode), the connection of both modules has to be made as low-inductive as possible in an converter phase.

Low-inductance DC-link power busbars are of special importance. This goes for the connection busbars of the capacitor battery itself as well as for connection of the power modules to the DC-link. In this respect, laminated busbar systems (tightly paralleled plate systems) adapted to the specific inverter layout have gained general acceptance in practice, achieving busbar inductances up to 20...50 nH. Some examples of this are shown in Figure 3.31.
The effects of the remaining inductances L_{11}+L_{12} on the power semiconductors can still be reduced by connecting C-, RC- or RCD-circuits directly to the DC-link terminals of the power modules. In most cases, a simple C-circuit with film capacitors within the range of 0.1...2 µF is connected.

Inductances of emitter or source

The elements L_{31} or L_{32} of the emitter/ source inductances are effective in the power circuit as well as in the driver circuit of the transistors.
Due to the fast di/dt of the transistor current, voltages will be induced which will have the effect of inverse feedback in the driver circuit (emitter/source inverse feedback). This, however, will decelerate the charging process of the gate-emitter-capacitance during turn-on and the discharging of the gate-emitter-capacitance during turn-off, resulting in increased switching times and switching losses.
The inverse feedback effect of the emitter may be utilized for limitation of the collector current di/dt in the case of short-circuits near the modules.
To minimize the inductances L_{31} and L_{32}, power modules are equipped with separate emitter control terminals.
If several BOTTOM driver stages of a converter are supplied by a common operating voltage with negative DC-link reference, the parasitic inductances between the ground connectors of the drivers and the negative potential of the DC-link may cause unwelcome oscillations in the ground loops. This problem can be solved by HF-stabilization of the driver operating voltage near to the output stage or separate supply voltage potentials of the BOTTOM driver stages in high-power inverters.

Inductance L_{21} and L_{22}

Inductances L_{21} or L_{22}, respectively, designate the inductance of the supply line between driver and transistor. Apart from increasing the impedance of the driver circuit, they may cause unwelcome oscillations with the input capacitance of the transistor. This may be remedied by a short, low-inductance connection between driver and transistor.

Capacitances

The capacitances C_{xx} in Figure 3.23 stand for the intrinsic capacitances in the power semiconductors (voltage-dependent, non-linear) and cannot be influenced by the user. They indicate the minimum value of the commutation capacitance C_K and, principally, effect a reduction of power dissipations during turn-off (see chapters 0 and 3.8).

Additional power dissipations are generated during active turn-on due to the recharge process of the commutation capacitances; these have to be considered in many high-frequency MOSFET-applications (...100 kHz...).
C_{11} and C_{12} cause an inverse dv/dt-feedback to the gate (Miller effect, see Figure 3.35).
In combination with the inductances near the switches, the intrinsic component capacitances may cause unwelcome oscillations.

3.4.2 EMI/mains feedbacks

3.4.2.1 Processes in the converter

Processes in a converter system will always produce unwelcome interference due to the switching operation of the power semiconductors on the one hand (Figure 3.24) and welcome energy transmission with the corresponding signal processing on the other hand.

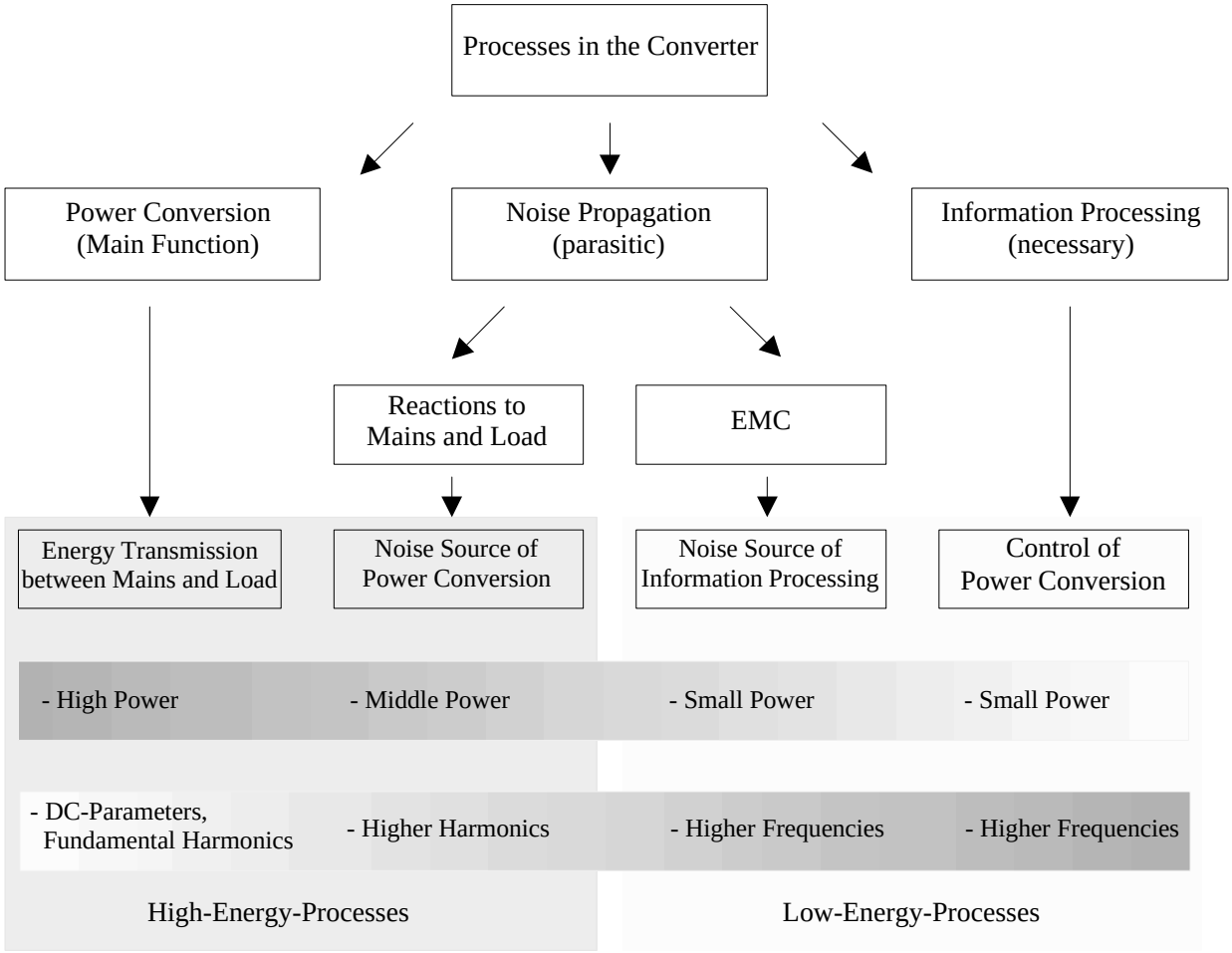


Figure 3.24 Energy processes in converters [299]

These processes can be divided up into high-energy-processes, which may cause interferences in the mains and the load within a frequency range between fundamental frequency and about 10 kHz, and low-energy-processes above 10 kHz up to about 30 MHz, where noise radiation and, consequently, non-conducted current flow will start to be propagated. The frequencies mentioned originate more or less from possible measuring procedures, and not from physical effects. In the low-frequency range, these effects are called converter mains feedbacks, which are

traditionally characterized by discrete harmonic current oscillations up to about 2 kHz. Above 10 kHz these oscillations are called radio interference voltages, which are indicated in dB/µV and are designated as interference voltages due to selective measurements. For the interim frequency range, within which modern power semiconductors are switched, the first attempts are currently being made to introduce measuring procedures as well as limit ratings. Discussions on these disturbing side-effects are contradictory, since the same physical processes are described under different aspects. The difference between designations such as zero current, leakage current or asymmetrical interference voltage is only given by various frequency range classifications and by the frequency dependency of all switching parameters. Since this frequency dependency is continuous just as the transition to radio interference, the frequency transition ranges are inevitably very broad.

3.4.2.2 Causes of interference currents

All interference is caused by the switching operation mode of power semiconductors. Causes of interference may be explained by the equivalent commutation circuit in Figure 3.25.

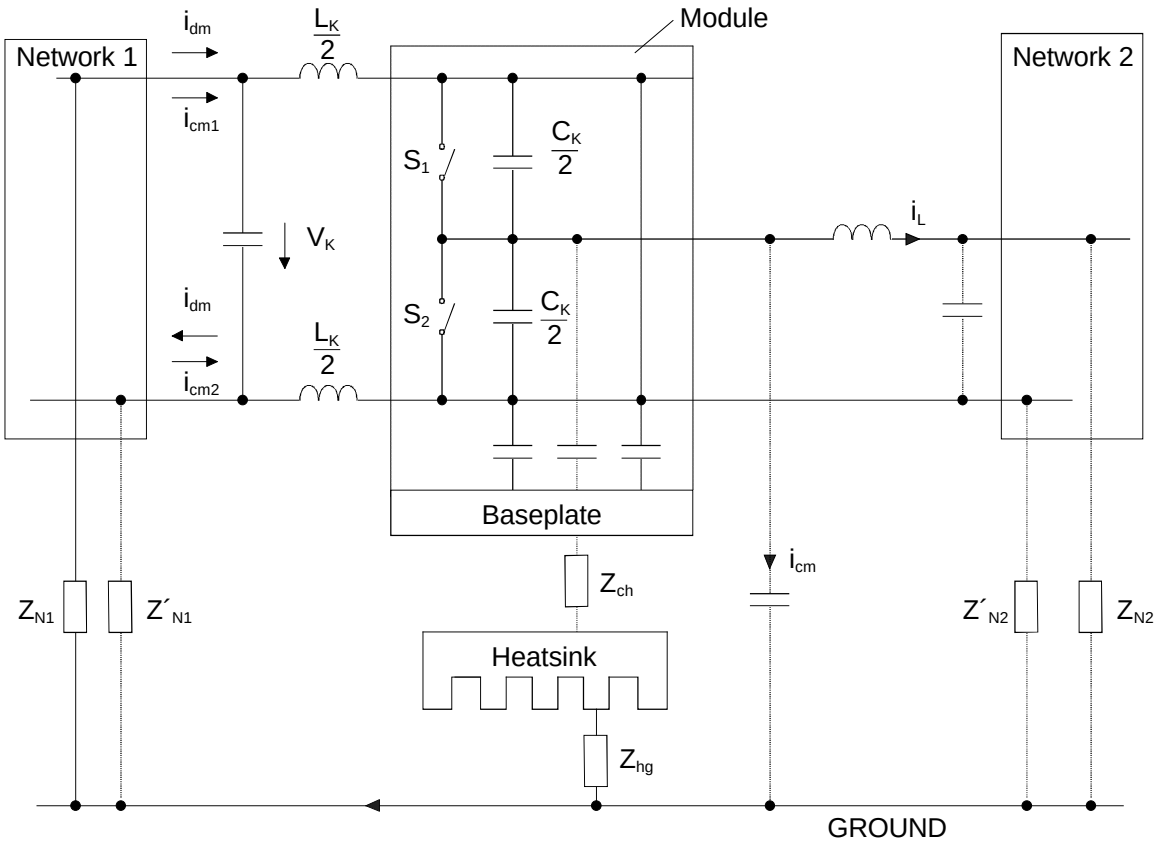


Figure 3.25 Equivalent commutation circuit with noise propagation paths [299]

In the case of *inductive commutation* switch S_1 will switch to the conducting switch S_2.
In a hard switching process ($L_K = L_{Kmin}$, $C_K = C_{Kmin}$) firstly the current will be commutated with a di/dt given by the semiconductor characteristics of switch 1. Commutation is finalized by the reverse-recovery-di/dt of switch 2, which determines voltage commutation and, consequently, dv/dt together with the current-carrying inductance and the effective capacitances C_K. The effective capacitances comprise all capacitances C_Σ which are effective towards the neutral potential. Together with the impedances of the commutation voltage connections to the neutral potential parallel impedances of the commutation capacitances will become effective. At the

beginning of the commutation process, the di/dt of switch 1 will cause a symmetrical current flow i_{dm} within the commutation voltage capacitance and the parallel network 1. The dv/dt at the end of the commutation process caused by the reverse-recovery-di/dt of switch 2 and the inductance L, which serves as supply current, conducts the currents i_{cm} asymmetrically via the ground line through the parallel lines to the commutation capacitances C_K.
Transition to soft turn-on by increase of L_K (ZCS, chapter 3.8) will reduce the di/dt and, consequently, symmetrical current interferences. At the same time, the increased inductances L_K will become effective in the circuit of the asymmetrical interference current. Dv/dt, at the beginning of the commutation process, is determined by the switching characteristics of S_1. The voltage leap at the end of the commutation process is determined by the reverse recovery current behaviour of switch S_2. Transition to soft switching in ZCS-mode will reduce current interferences and will change the frequency range of asymmetrical currents, without reducing them considerably, also see chapter 3.8.3.

The *capacitive commutation process* is started by active turn-off of switch S_1.
In the hard switching procedure ($C_K = C_{Kmin}$) the asymmetrical interference current is determined by the impedances towards the neutral potential which become effective parallel to the commutation capacitances and by the semiconductor characteristics of switch S_1. The current commutation following the voltage commutation and, thus, the symmetrical interference current is determined by the turn-off behaviour of S_1 and by the turn-on behaviour of S_2.

An increase of C_K will require a zero-voltage-switch with soft turn-off (chapter 3.8). The turn-off process starts with the first stage of current commutation with a di/dt, that is determined by switch S_1 at a reduced voltage. The delayed dv/dt will reduce the asymmetrical currents during voltage commutation. Passive turn-on of S_2 determines the di/dt during the second stage of current commutation. Asymmetrical current interference will be reduced by soft switching in ZVS-mode without changing symmetrical currents noticeably. Nevertheless, the increased capacitances C_K will diminish the symmetrical interference current in network 1 in relation to the capacitive current divider. Soft switching converter circuits with turn-on or turn-off phase-shift control will reduce asymmetrical and symmetrical interference currents when using zero-voltage switches or zero-current switches, respectively. In converter circuits with auxiliary commutation arms, where ZVS and ZCS are switched alternately, interference currents will not be reduced considerably in comparison to hard switching circuits, see chapter 3.8.3.

3.4.2.3 Propagation paths

In order to take measurements on radio interference voltages, voltage fluctuations at the mains connections of inverter to ground are selectively measured. The potential fluctuations refer to a defined point of ground, which is determined in standard measurements by connection of a line impedance stabilization network. Regarding symmetrical and asymmetrical interference currents within the frequency range of EMI, all simple low-frequency switching elements are equipped with additional inductances, resistances and capacitances, which will render a clearer simulation of their frequency dependency.

Figure 3.26 shows the example of a simple step-down converter circuit, where network 1 is represented by the line impedance stabilization network (LISN) and network 2 by the applied load in contrast to Figure 3.25.

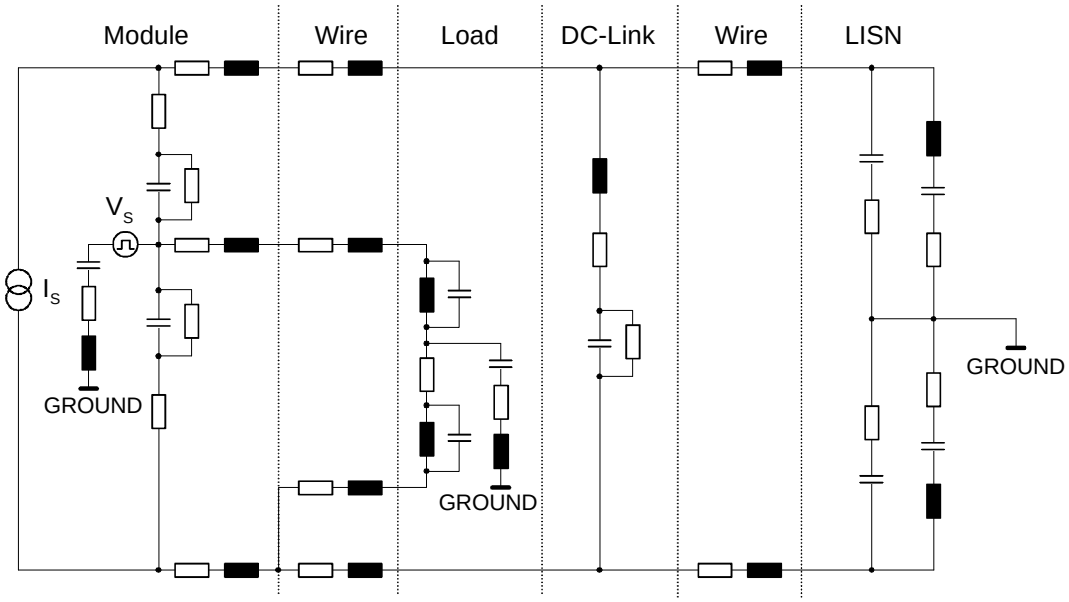


Figure 3.26 EMI-equivalent circuit of a step-down converter [193]

The module simulates switches S_1 and S_2 including the commutation inductances and capacitances. The origins of interference currents described beforehand are illustrated in a simplified way, namely as current source I_S for symmetrical interference currents and as voltage source V_S for asymmetrical interference currents. In both sources the measured semiconductor characteristics are included as a function of time (Figure 3.27).

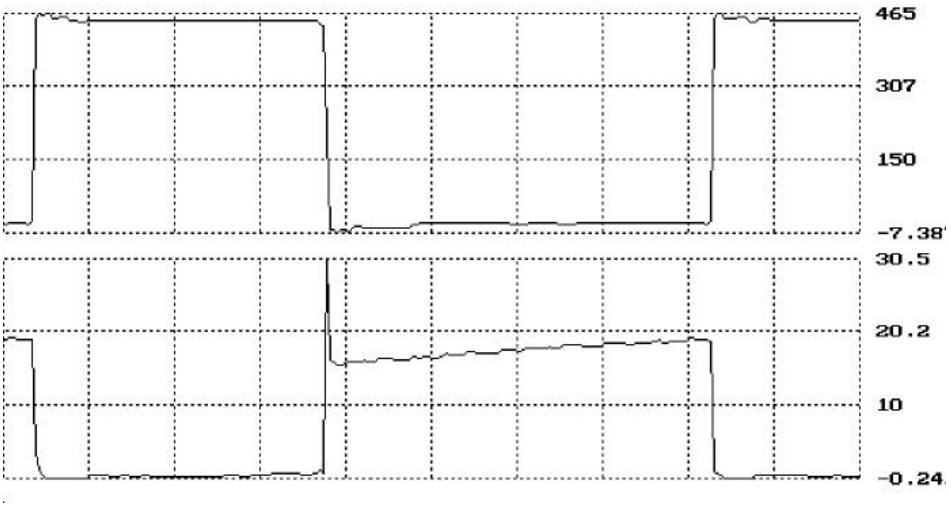


Figure 3.27 Typical voltage and current characteristics of an IGBT-switch (top characteristic in V, bottom in A) [193]

Figure 3.28 shows simulated results with the example taken from [193] based on the model of Figure 3.26; these results are almost fully in accordance with the measurements actually taken.

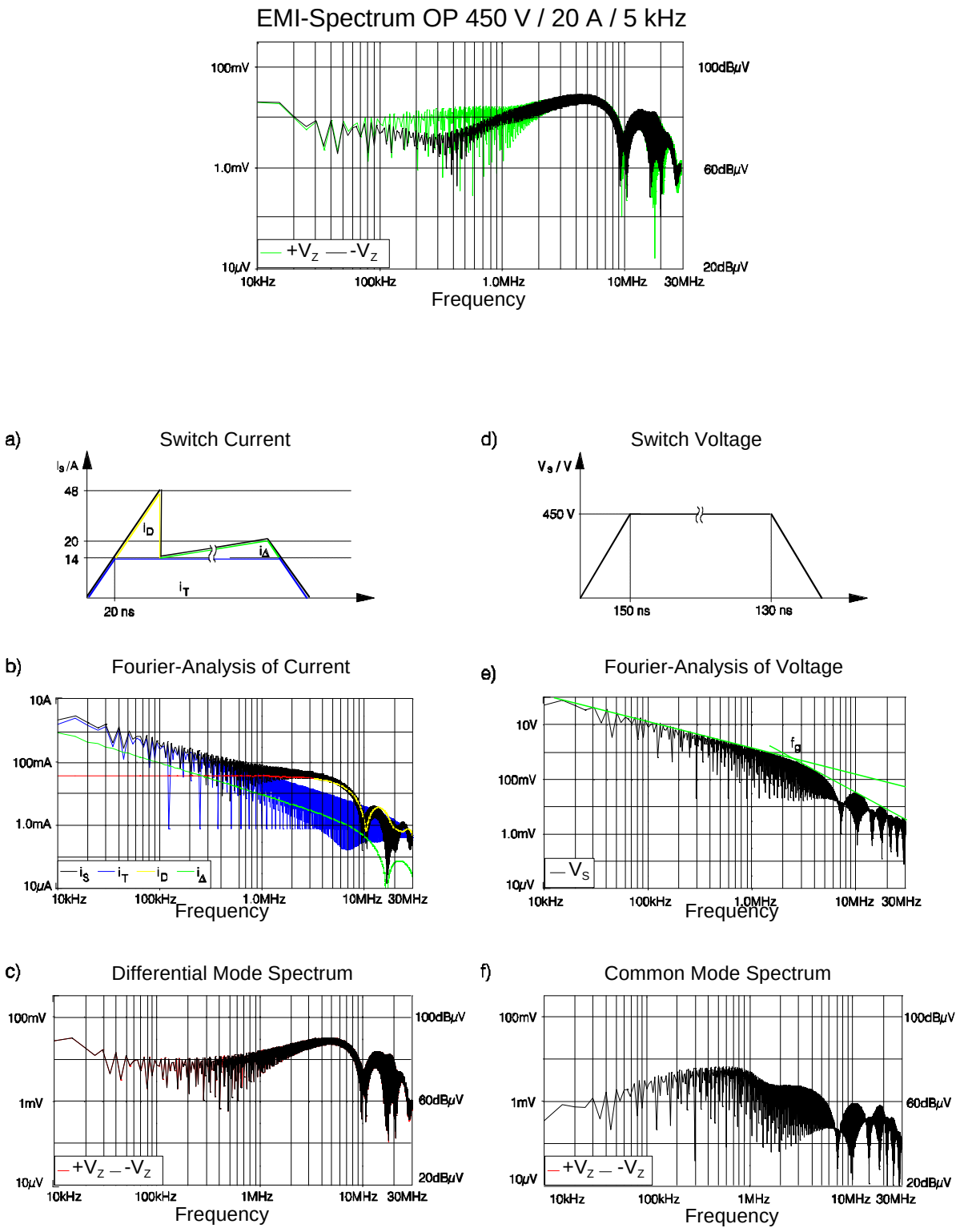


Figure 3.28 Simulation results of a 1200 V/50 A – NPT – IGBT dual module
Operation parameters: DC-link voltage V_{DC} = 450 V
Load current = 20 A
Pulse frequency = 5 kHz

The influence of additional paths of propagation via energy and information transmission lines of the driver circuits have been examined in [299].

3.4.2.4 EMI suppression measures

Conventional interference suppression is based on the use of customised filters, which are attached to the mains supply of the device. According to the set limit characteristics for a certain type of device (see example tables) various filters are applied by means of the line impedance stabilization network and standardized test assemblies, until the limit values are kept in all frequency ranges [259].

Table of engineering standards

GENERIC	Engineering standard	Application	Interference factor
EN 50 082/1	VDE 0839, part 82-1	Residential, commercial and trade applications, small businesses	EMI immunity
EN 50 081/1	VDE 0839, part 81-1		Interference emission
EN 50 082/2	VDE 0839, part 82-2	Industry, power stations etc.	EMI Immunity
EN 50 081/2	VDE 0839, part 81-2		Interference emission

Examples for existing product standards

Classification of equipment	Product Standards	Interference factor
ISM-devices (industrial, scientific and medical HF-devices)	EN 55 011	Interference emission
	Generic EN 50 082-1/2	EMI immunity
Radio and television receivers and connected equipment	EN 55 013	Interference emission
	EN 55 020	EMI immunity
Household appliances	EN 55 014	Interference emission
	Generic EN 50 082-1	EMI immunity
Fluorescent lamps and lights	EN 55 015	Interference emission
	Generic EN 50 082-1	EMI immunity
Data processing systems	EN 55 022	Interference emission
	prEN 55 101, EN 55 024	EMI immunity

In this mostly empirical procedure, often costly filters are used. It will be more effective to design and construct a circuit, which considers, from the beginning of any development processes, the effects of electromagnetic interference and the optimization of propagation paths with respect to their origins and to possible measuring points. Optimization means either to produce high-resistance propagation paths for interference currents by the application of selective blocking circuits or to create low-resistance short-circuit paths for interference currents by using selective suction filter circuits.
In the following, selected measures are explained with regards to Figure 3.25.
Symmetrical interference current circuits will be closed via the capacitance of the commutation voltage source. Ideal capacitance connected to switches 1 and 2 without the influence of any line impedances would be required for the creation of a short-circuit path for interference currents. Measurable radio interference voltages will then be generated via the capacitive voltage ripple, which will effect a current flow over the paralleled effective circuits. Therefore, all measures that may be taken to reduce symmetrical inerference currents will aim at the arrangement of corresponding suction filter circuits parallel to the connection lines of the commutation voltage. All efforts in this respect can be reduced in relation to which extent the creation of a filter circuit as near as possible to the switch connections may be achieved by nearly ideal capacitances and active filters.
Principally, asymmetrical interference currents will be propagated via the ground line. For interference suppression it seems to be important to have extremely high-resistance impedances

in all switching points with steep potential increases versus ground potential and, at the same time, to limit the jumping potential to the non-avoidable switch connections. In the example of the equivalent circuit in Figure 3.25, firstly, interference suppression could be managed by reduced coupling capacitances of the drivers and capacitances effective via the module base plate and the heatsink. If the drivers do not receive switching information and are not supplied with auxiliary energy by the neutral potential, no shifted currents will be conducted via the earth line, i.e. the circuit will be closed within the appliance. There will be no flow of asymmetrical interference currents. Interference currents propagating over the base plate may be reduced by applying shielding measures and different isolation materials [193]. With application of the measures mentioned above (near to the semiconductor chips) a considerable reduction of interference currents can be achieved, as shown in Figure 3.29 with the example of an especially modified IGBT module [193].

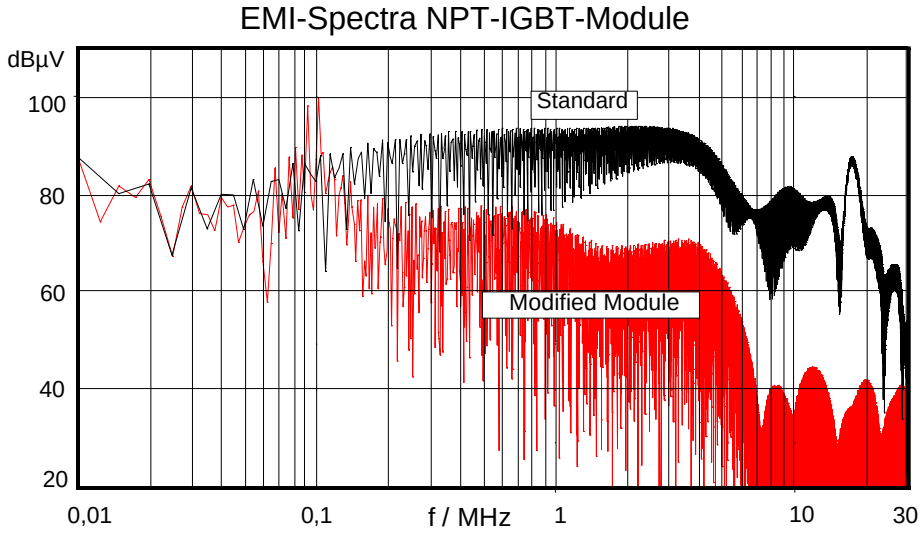


Figure 3.29 Comparison of interference spectra of a standard IGBT module and an EMI-optimized IGBT module; [193];
Operation parameters: DC-link voltage = 450 V
Load current = 20 A
Pulse frequency = 5 kHz

The connection to network 2 via the choke coil depicted in Figure 3.25 is not influenced by these measures. The coupling capacitance of this connection line can only be reduced by shortening the line as far as possible. Ideally, an L/C filter should be connected directly to the the jumping potential so that the inductance of which will attenuate the potential jumps to such an extent that all other coupling capacitances in network 2 will not be able to contribute considerably to the asymmetrical interference current. If network 2 is the supply point of the mains where the standard measurement using LISN is done then this measure will be inevitable, i.e. the L/C filter has to be part of the EMI filter.

3.4.3 Power units ready for installation

SEMIKRON offers power units ready for installation both in module and MiniSKiiP or SKiiP product range, which are designed according to the above mentioned standards and optimized with respect to the characteristics of the applied power modules.

The functional spectrum may comprise
- input rectifiers with diodes, thyristors or transistors,

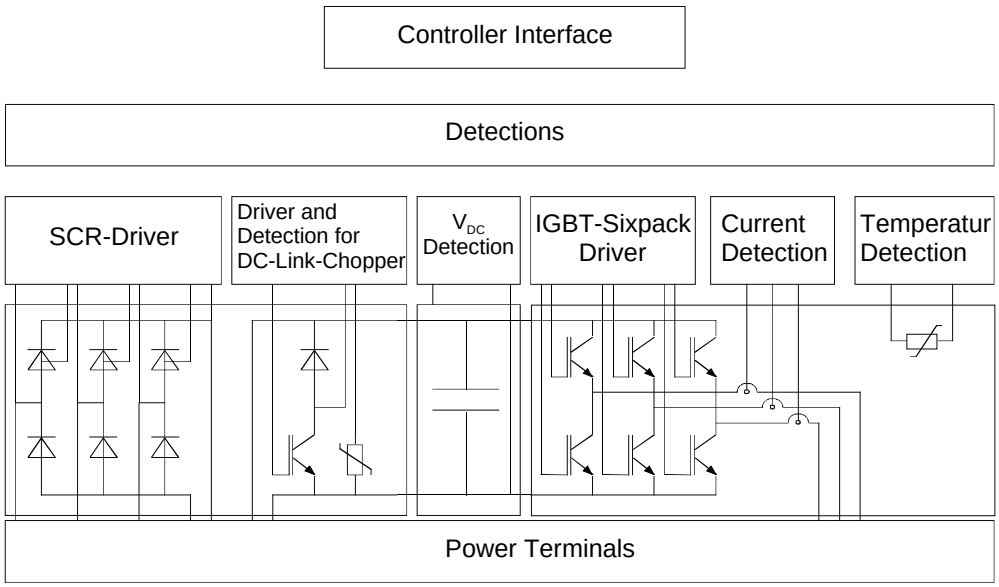
- laminated DC-links with Cu- or Al-sandwich busbars, electrolytic or film capacitors, HF-blocking capacitors, balancing and discharge resistors,
- inverter legs with IGBT or MOSFET modules or SKiiPPACKS,
- liquid coolant or forced air heatsinks; fan optional,
- driver with protection functions, sensors, power supply and potential isolation.

Before delivery, all power units have to pass application-specific functional testing.

Powerboards with MiniSKiiP

Figure 3.30 shows view and block diagram of a SKiiP025HAB powerboard with MiniSKiiP 8 layout for up to 15 kW power output at a line supply voltage of 400 V .

a)



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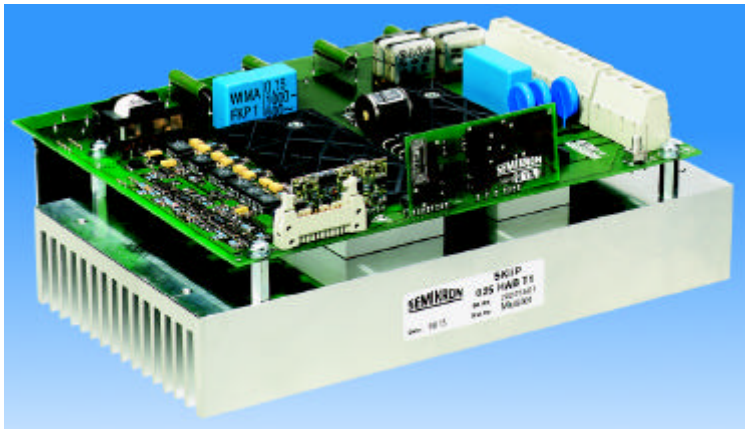


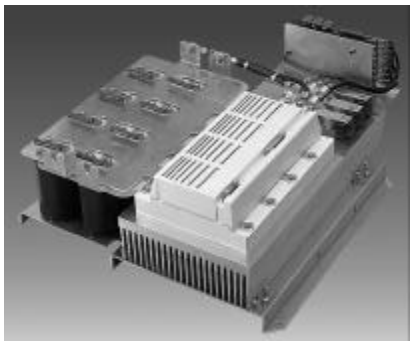
Figure 3.30 Powerboard SKiiP 025HAB/NAB
a) Block diagram b) View (without fan)

MiniSKiiPs SKiiP 83 ANB15 (diode rectifier and brake chopper / version NAB) or SKiiP AHB15 (half-controlled thyristor rectifier and brake chopper / version HAB) as well as SKiiP 83 AC12I (three-phase inverter with IGBTs 120A @ 25°C and AC current sensors), DC-link (700 µF), potential-separated driver, power supply, overcurrent, overtemperature and undervoltage protection and a DC-link charge circuit (for version HAB) are integrated into a central PCB of the powerboard.

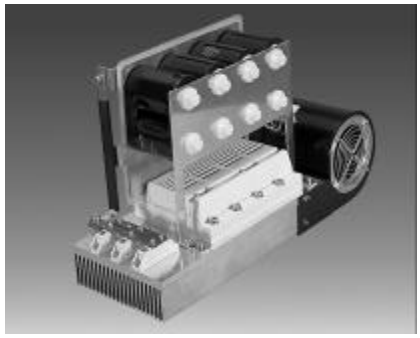
The PCB is mounted on to the heatsink via the MiniSKiiP components and additional support pins.

SKiiP power units

SKiiP power units are equipped with one or several integrated SKiiPPACKs (also connected in parallel), a sandwich DC-link and optional rectifiers, fans and additional snubber circuits, if required by the customer.
Figure 3.31 shows different SKiiP-types with vertical or horizontal DC-link construction.



a)



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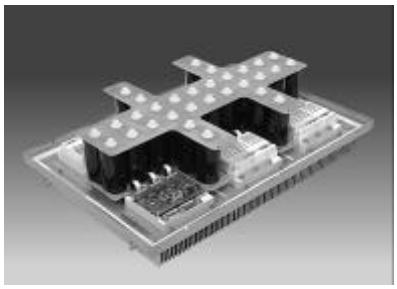


c)

Figure 3.31 Construction types of SKiiP power units
a) Flat construction for wide switchboards
b) Vertical standard DC-link
c) SKiiP-RAC with IGBT rectifier and converter

For power supply voltages from 230V up to 690V all available SKiiPPACKs may be integrated into SKiiP power units. Power outputs up to MW-range may be produced by paralleling SKiiPPACKs, using either SEMIKRON standard heatsinks or, optionally, nearly any other forced air or liquid coolant heatsinks supplied by the customer.

Figure 3.32 shows the example of a SKiiP power unit for a rectified 690 V mains (DC-link voltage up to 1200 V), comprising 3 SKiiPPACKs SKiiP 1092GB170-474 CTV with fibre optic inputs, a sandwich DC-link construction totalling up to 8.8 mF /1350 V and a radial fan. At a pulse frequency of 3 kHz and a supply air temperature of 35°C the effective output current (50 Hz) will value up to 250 A during continuous operation and to 375 A for operation period of 1 min/10 min.

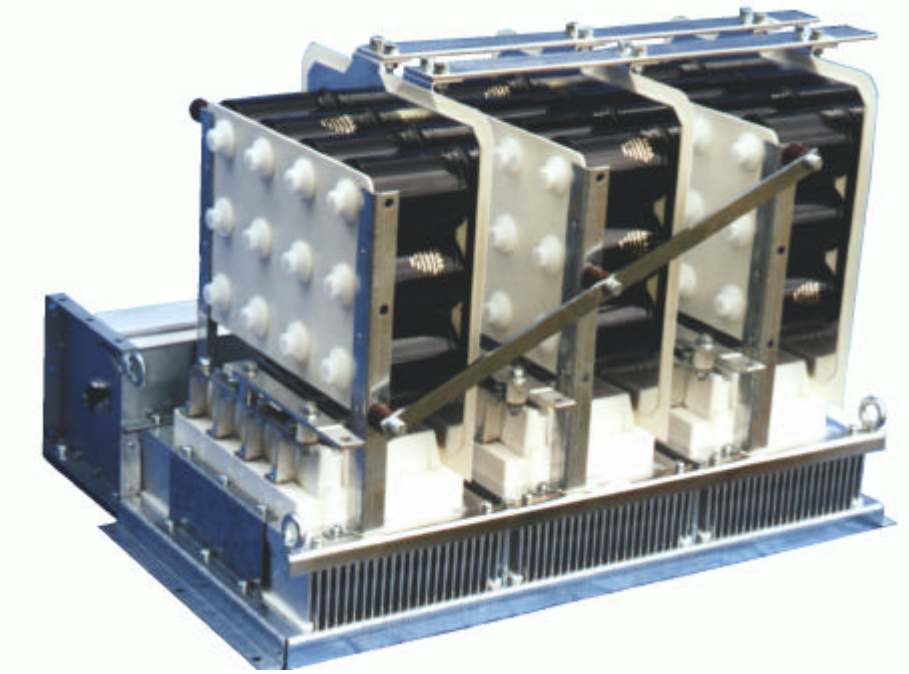


Figure 3.32 300 kVA inverter unit with SKiiPPACKs

Power units with SEMITRANS IGBT- or MOSFET-modules

For applications, where SKiiPPACK or MiniSKiiP power units will not be sufficient, assemblies with SEMITRANS modules, SEMIDRIVERs, standard heatsinks and laminated DC-links may be a solution. These can also be subjected to application-specific testing, if required.

The power units described above, which are characterized as sub-systems by nature, require a different dimensioning by user and manufacturer compared to modules.
In this respect, SEMIKRON offers their calculation programme SKiiPsel to SKiiP and MiniSKiiP customers as a tool for pre-selection and rough dimensioning, see chapter 3.10.2.
Further steps may then be co-ordinated by means of a “checklist”, which should consider, among other things, the following technical aspects:

- application, power flow direction(s), circuit structure, required functions,
- mounting dimensions (size, weight), special requirements (oscillations, shock load, etc.),
- input (mains, generator, battery,etc.), input voltage range, cos φ, special requirements; for mains feedback: fundamental frequency, pulse frequency, DC-link voltage,
- output (mains, transformer, DC-motor, AC-motor, reluctance motor, etc.), output voltage range, output current, cos φ , overload (value/duration/frequency), fundamental frequency (min./max.), current at min. fundamental frequency, pulse frequency, load cycles (current, voltage, frequency, cos φ as a function of time),
- DC-link (electrolytic or film capacitors), rated voltage, min./max. capacitance, max. DC-link voltage, ambient DC-link temperature,
- isolation test voltages, type of protection,
- driver, driver interface (transformer, optical), options (sensors for current, temperature, DC-link voltage),
- cooling: ambient temperature/coolant temperature min./max; for natural air cooling: max. air volume, admissible noise level,
- for liquid cooling: cooling medium (antifreeze, volume, rate of flow),

- storage temperature, special requirements with respect to climate, extreme altitude over NSL,
- required module life (power modules, DC-link capacitors).

3.5 Driver

3.5.1 Gate voltage and gate current characteristics

Driving process

As already described in chapter 1.2.3 the switching behaviour of MOSFET and IGBT modules can be greatly controlled by recharge the gate capacitance.
In theoretical borderline cases, the gate capacitance recharge may be controlled by resistance, voltage or current (Figure 3.33).

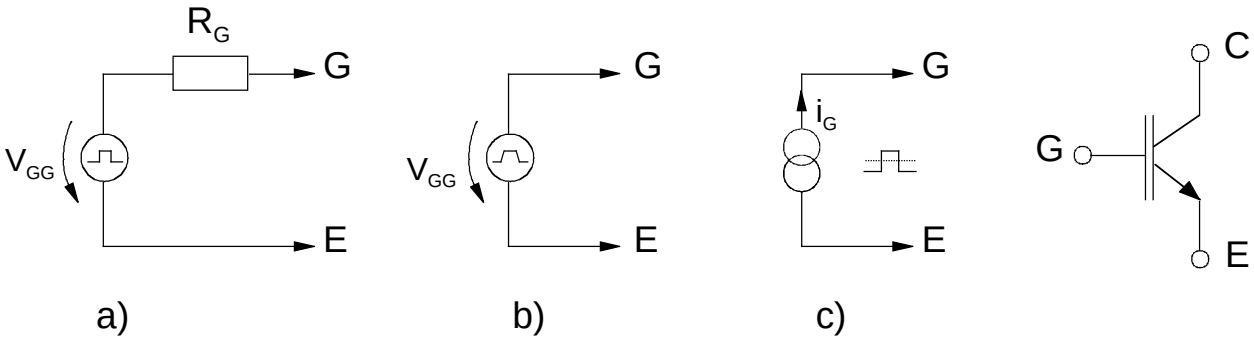


Figure 3.33 Gate driving process for MOSFETs and IGBTs [194]
a) Control by resistance b) Control by voltage c) Control by current

The preferred variant is to drive the system via a gate resistor (or two separate resistors for turn-on and turn-off) according to Figure 3.33a. Characteristic of this variant is the Miller plateau in the gate-source or gate-emitter voltage, respectively (Figure 3.34). The switching speed is adjusted by R_G at a continuous supply voltage V_{GG}; the smaller the R_G, the shorter the switching times. The disadvantage of resistance control is that the gate capacitance tolerances of the MOSFET or IGBT will have direct influence on switching times and switching losses.
Impressed voltage at the transistor gate driven according to Figure 3.33b will eliminate this influence; the switching speed of the transistor is directly determined by the gate dv/dt. Thanks to this voltage no Miller plateau will be formed in the gate voltage characteristic. This requires sufficient driver current capacity.
Current control by a “positive“ and “negative“ gate current generator, as shown in Figure 3.33c, determins the gate charge characteristics (see Figure 1.12 and Figure 1.13) and is comparable to resistance control with respect to gate voltage characteristics.

Control voltage ratings

Figure 3.34 shows the characteristics for gate current i_G and gate-emitter voltage v_{GE} in a resistance controlled circuit.

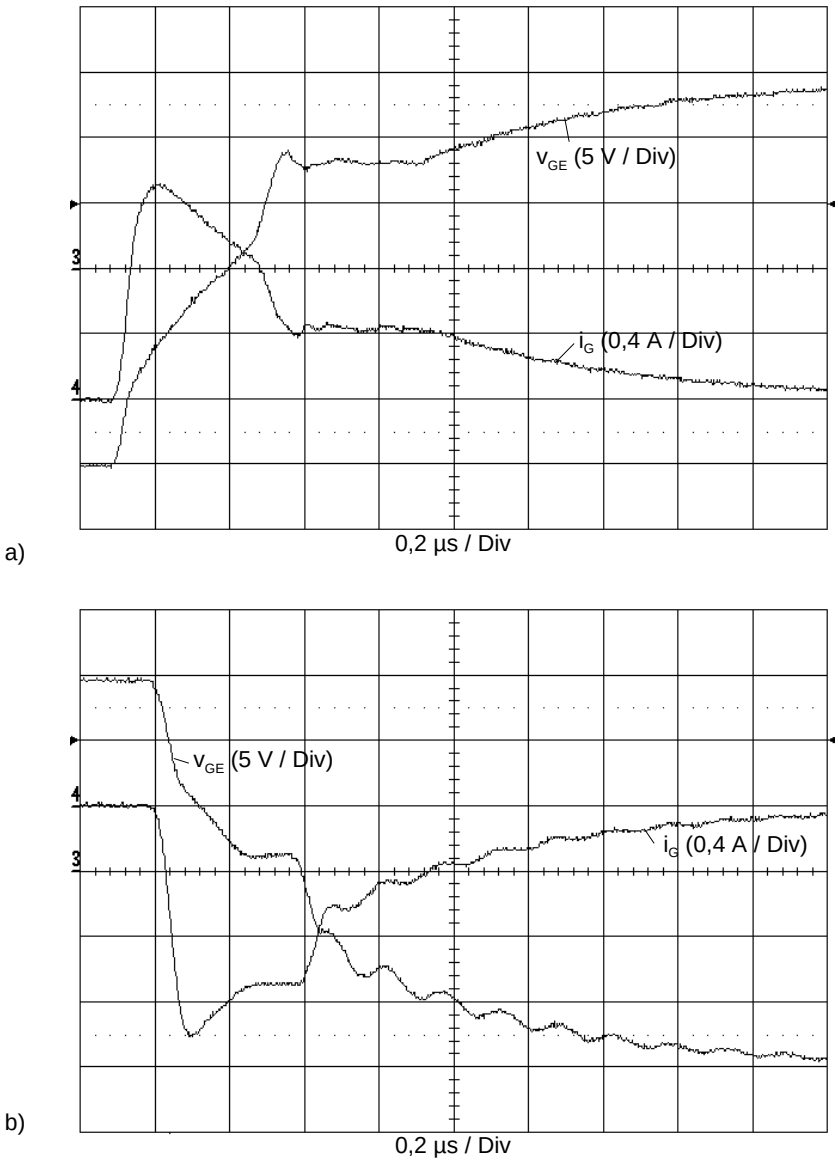


Figure 3.34 Gate current and voltage characteristics during turn-on and turn-off
a) Turn-on b) Turn-off

The control voltage V_{GG} for both polarities has to be dimensioned according to the electrical strength of the gate isolation, which is usually indicated as 20V for current power MOSFETs and IGBTs. This value may not be exceeded - not even transiently - which might require special measures during turn-off, see chapter 3.5.2 and 3.6.3.2.
On the other hand, $R_{DS(on)}$ and V_{CEsat}, respectively, will decrease when the gate voltage increases, and, therefore, we recommend applying a positive control voltage, which delivers a gate voltage of

V_{GS} = +10 V for power MOSFETs and
V_{GE} = +15 V for IGBTs

during stationary on-state. Most datasheet ratings are based on these measuring parameters.

As demonstrated in Figure 3.34, the gate voltage for IGBTs should be negative to the emitter potential during turn-off and off-state; recommended values are -5...-8...-15 V.

This will maintain a negative gate current during the complete turn-off procedure (even if V_{GE} approaches $V_{GE(th)}$) sufficiently to draw the main share of positive charge carriers from the n^--drift zone by means of a high dv_{CE}/dt during turn-off time and, thus result in a short tail current.
Another, more serious disadvantage of blocking the IGBTs of a bridge circuit with V_{GE} = 0 V will occur during the reverse-recovery of the parallel inverse diode of the turned off transistor because of the dv_{CE}/dt (Figure 3.35).

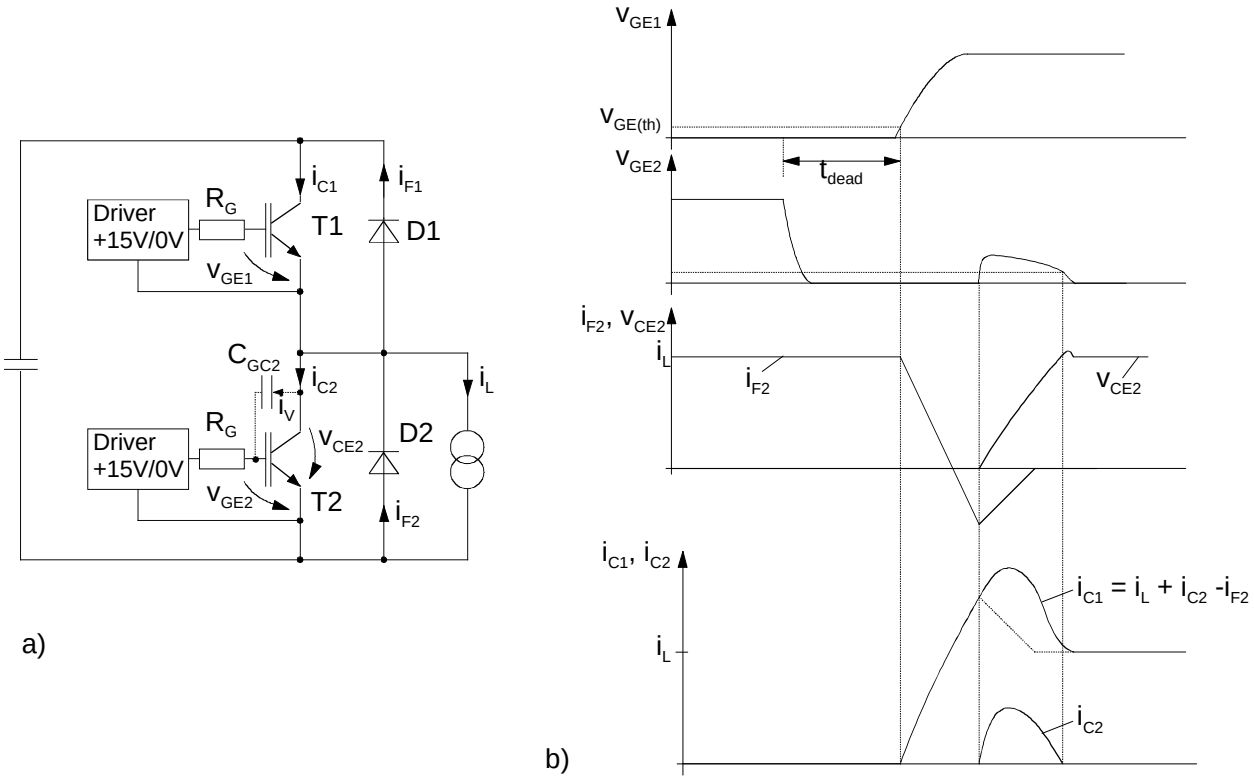


Figure 3.35 Cross current in an IGBT bridge arm due to turn-on by dv_{CE}/dt-feedback of T_2
a) Switching principle b) Current and voltage characteristics

The high dv_{CE}/dt of the collector-emitter voltage v_{CE2} during the reverse-recovery-di/dt of D_2 will effect a displacement current i_V through the gate-collector capacitance C_{GC2}, also see chapter 1.2.3

$i_V = C_{GC} * dv_{CE}/dt.$

This displacement current, in turn, will cause a voltage drop over the resistance R_G (or R_{GE}/R_G). If, as a result of this, v_{GE} rises and exceeds the threshold voltage $V_{GE(th)}$, T_2 will be driven to its active region during the reverse-recovery-di/dt (cross current, additional power dissipation in T_1 and T_2).

Other than with IGBTs, the application of a stationary negative gate-source voltage during off-state is not recommended for driving power MOSFETs. Parasitic turn-on with all consequences, as described above, is done within the MOSFET too at the same time. However, it will protect the transistor structure of the MOSFET, which is only limited resistant to dv/dt. The equivalent circuit of a power MOSFET (Figure 1.3) demonstrates the displacement current through C_{DS} to the base of the parasitic npn-bipolar transistor as a result of dv_{DS}/dt. If the voltage drop at the lateral p-well-resistor R_W reaches threshold voltage level, the bipolar transistor will be turned on parasitically, which may lead to destruction of the MOSFET by power dissipation during periodic operation.

Parasitic turn-on of the MOSFET channel at V_{GS} = 0 V over C_{GD} will reduce dv_{DS}/dt during blocking state and will weaken the dangerous effect of bipolar transistor turn-on (see Figure 3.35).

Control current ratings, driving power

The total driving power P_{Gavg} to be delivered by the driver circuit can be determined from the gate charge Q_{Gtot} (see Figure 1.12 and Figure 1.13):

$$P_{Gavg} = \left(V_{GG+} + \left|V_{GG-}\right|\right) \cdot Q_{Gtot} \cdot f_s \qquad \text{with } Q_{Gtot} = C_{Equiv.} \cdot \left(V_{GG+} + \left|V_{GG-}\right|\right)$$

Peak gate current values are calculated as follows:

$$I_{GMon} = \left(V_{GG+} + \left|V_{GG-}\right|\right) / R_{Gon} \qquad \text{(ideal)}$$

$$I_{GMoff} = \left(V_{GG+} + \left|V_{GG-}\right|\right) / R_{Goff} \qquad \text{(ideal)}$$

Driver power is calculated as follows:

$$P\left(V_{GG+}\right) = V_{GG+} \cdot Q_{Gtot} \cdot f_s \qquad f_s = \text{switching frequency}$$

$$P\left(V_{GG-}\right) = \left|V_{GG-}\right| \cdot Q_{Gtot} \cdot f_s$$

Example: V_{GG+} = 15 V, V_{GG-} = -15 V, R_G = 3.3 Ω
Q_{Gtot} = 2.3 µC (SKM500GB123DS)
f_s = 10 kHz, V_{DC} = 600 V

Resulting in: $I_{GMon} = \left|I_{GMoff}\right| = 9.09\,A$
$P_{Gavg} = 0.69\,W$
$P\left(V_{GG+}\right) = P\left(V_{GG-}\right) = 0.345\,W$
$I\left(V_{GG+}\right) = I\left(V_{GG-}\right) = 23\,mA$ (average)

3.5.2 Influence of driver parameters on switching features

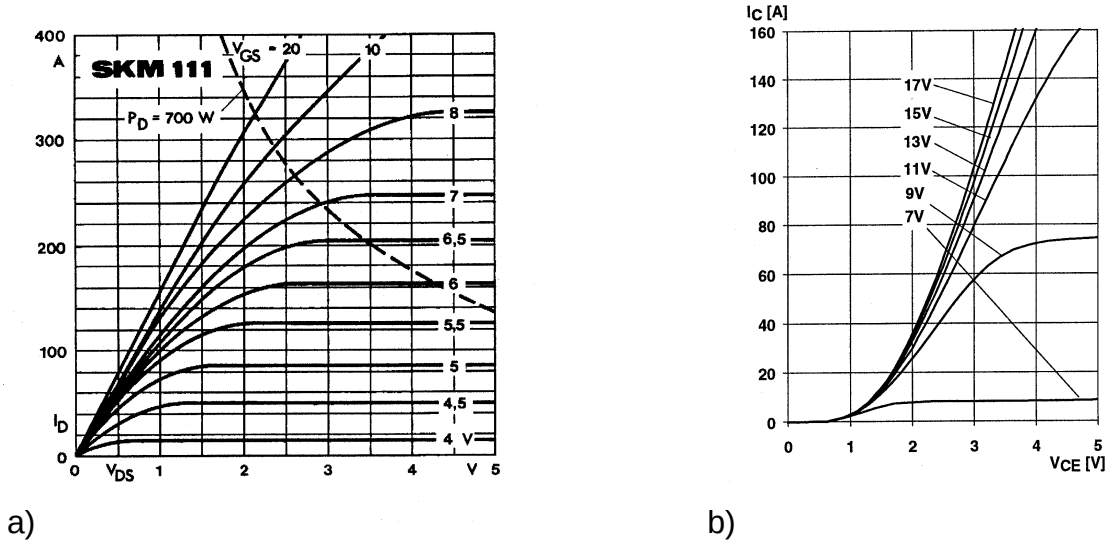
As already mentioned, important features of driven power MOSFETs or IGBTs are dependent on V_{GG+}, V_{GG-} and R_G ratings. The following table shall give a first overview (<: increases, > decreases, -: remains):

Rating/ characteristic	V_{GG+} <	$\left\|V_{GG-}\right\|$ <	R_G <	see chapter
$R_{DS(on)}$, V_{CEsat}	>	-	-	3.5.2
t_{on},	>	<	<	3.5.2
E_{on}	>	-	<	3.5.2
t_{off}	<	>	<	3.5.2
E_{off}	-	>	<	3.5.2
turn-on peak current *)	<	-	>	3.5.2
turn-off peak voltage *)	-	<	>	3.5.2
dv/dt-sensitivity (MOSFET)	<	<	>	3.5.1
(IGBT)	<	>	<	3.5.1
actively limited I_D, I_C	<	-	<	3.6.2
ruggedness to load short-circuits	>	-	<	3.6.2

*) during hard switching under ohmic-inductive load

Forward characteristics ($R_{DS(on)}$, V_{CEsat})

The dependences of the forward characteristics of power MOSFETs and IGBTs on the drive parameters can be read from their output characteristics (see chapter 1.2.2). In Figure 3.36 this is explained with one example each for SEMITRANS-MOSFETs and IGBTs taken from the current datasheets.



a) b)

Figure 3.36 Forward characteristics versus control voltage (gate voltage)
a) Power MOSFET-module SKM 111
b) IGBT-module SKM100GB123D

In SEMITRANS, SEMITOP and MiniSKiiP datasheets the recommended maximum ratings and characteristic values mentioned in chapter 3.5.1 are indicated with V_{GG+} = 10 V for power MOSFETs and V_{GG+} = 15 V for IGBT modules which is an acceptable compromise in conventional applications between power dissipations, turn-on peak current and short-circuit behaviour.

Switching times, switching losses (t_{on}, t_{off}, E_{on}, E_{off})

Control voltages and gate resistances will affect the various parts of turn-on time $t_{on} = t_{d(on)} + t_r$, turn-off time $t_{off} = t_{d(off)} + t_f$ and tail time t_t of the IGBT in different ways:
Since the gate capacitance amounts to absolute ratings of V_{GG+} and V_{GG-} before switching, the recharge time will decrease (turn-on delay time $t_{d(on)}$, turn-off delay time $t_{d(off)}$) on condition of a given gate resistor R_G if the recharge current or ($V_{GG+} + |V_{GG-}|$) increases.
On the other hand, switching times t_r and t_f and, consequently, energy dissipations E_{on} and E_{off} may only be affected by the switching control voltages V_{GG+} or V_{GG-}, since they determine the current flow through the gate resistor R_G.

SEMITRANS-IGBT datasheets include diagrams showing the dependences of switching times and energy dissipations on R_G, measured for maximum current ratings I_C @ 80°C on condition of hard switching under ohmic-inductive load (Figure 3.37).

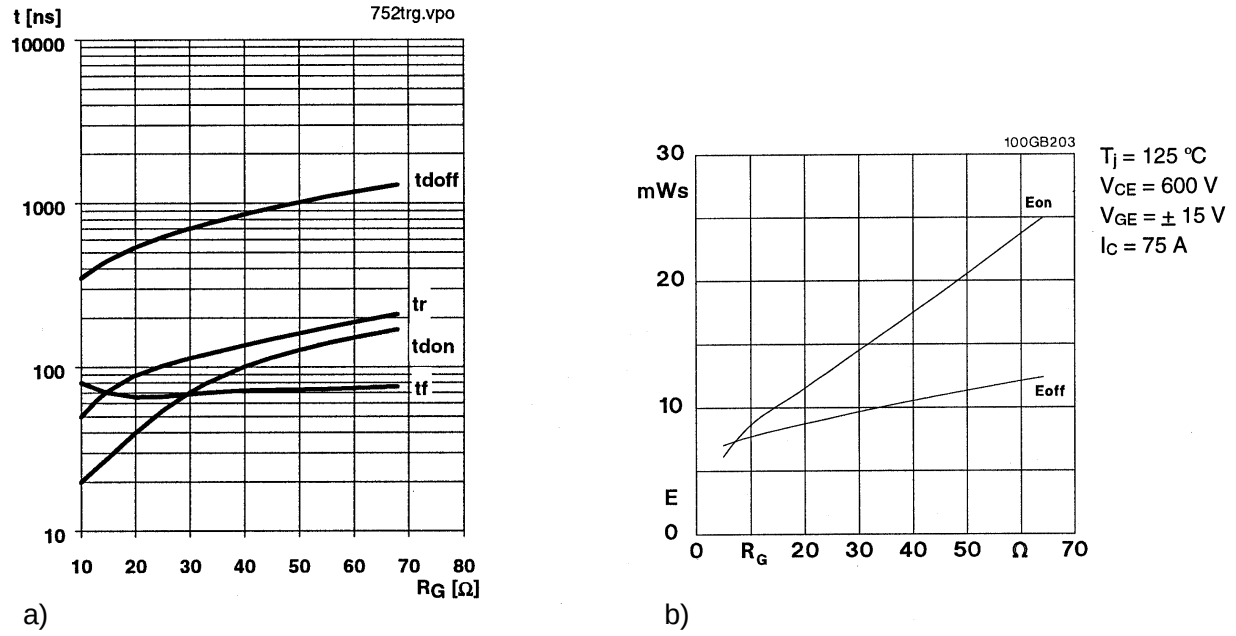


Figure 3.37 IGBT-switching times (a) and switching losses (b) of SKM100GB123D versus gate resistor R_G at T_j = 125°C, V_{CE} = 600 V, I_C = 75 A, V_{GE} = ± 15 V and on condition of hard switching under ohmic-inductive load

Switching behaviour of free-wheeling diode and turn-on peak current of transistor

The turn-on energy dissipation of the IGBT indicated in Figure 3.37b already includes the influence of the turn-off behaviour of the integrated free-wheeling diode on turn-on peak current and turn-on power dissipations, see chapters 1.3.3.3 and 2.3.3.

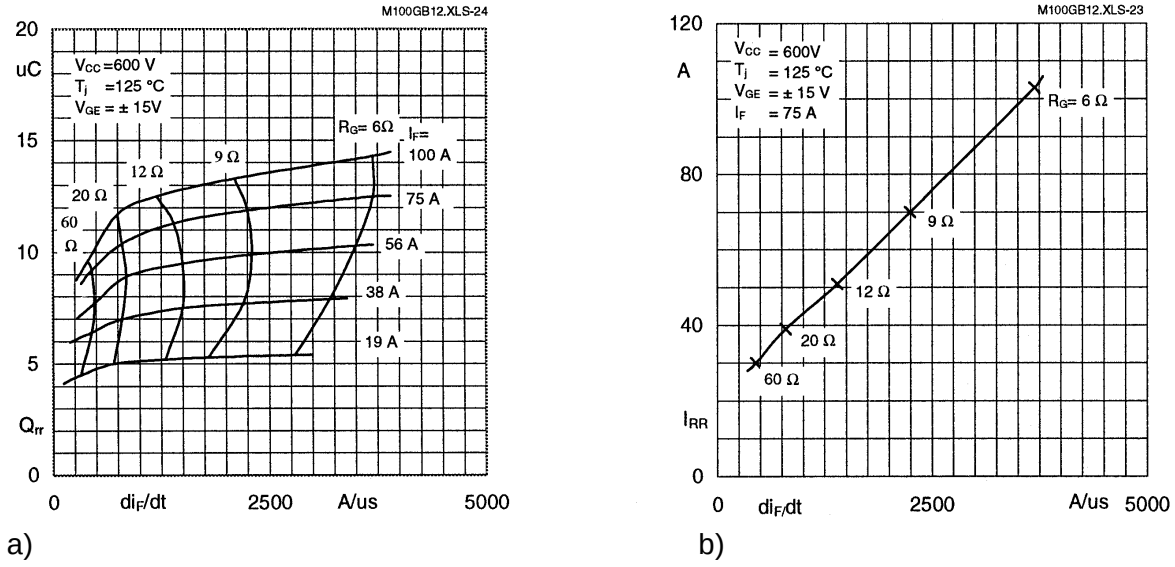


Figure 3.38 SKM100GB123D CAL-diode recovered charge Q_{rr} (a) and peak reverse recovery current I_{RRM} (b) versus commutation speed di_F/dt of diode current

The drain or collector current (i_D, i_C) rise time t_r will decrease with rising gate current (higher V_{GG+} or lower R_G). This in turn will increase the current commutation speed di_F/dt in the free-

wheeling diode, by which recovered charge Q_{rr} and peak reverse recovery current I_{RRM} are determined.
These characteristics of CAL-diodes used in SEMITRANS-IGBT-modules are depicted in the datasheets (Figure 3.38 and 3.39).
Increase of Q_{rr} and I_{RRM} will cause higher turn-off power dissipations in the internal free-wheeling diode.
Since a higher di_F/dt will result in an increase of Q_{rr} and I_{RRM} and, since I_{RRM} is added to the load current within the collector or drain current, turn-on peak current and turn-on energy dissipation of the transistor will increase with its turn-on speed (Figure 3.37).

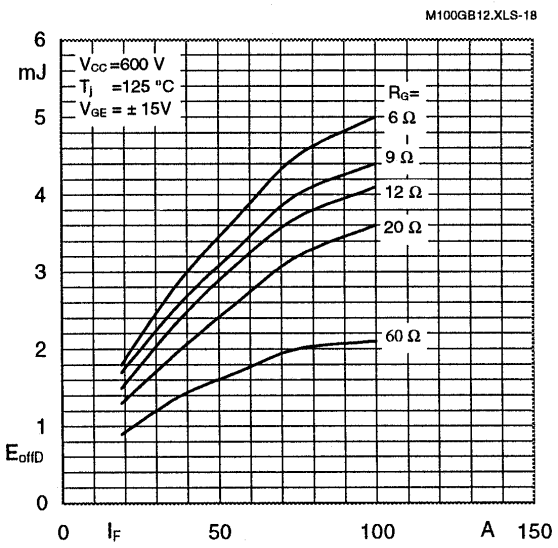


Figure 3.39 CAL-diode turn-off energy dissipation E_{offD} in a SEMITRANS IGBT-module SKM100GB123D versus R_G

Turn-off peak voltage

If either V_{GG-} is increased or R_G is decreased, the turn-off gate current of the driven transistor will rise. As shown in Figure 3.37a, the drain or collector-current fall time t_f will decrease, i.e. $-di_D/dt$ or $-di_C/dt$ will increase. The voltage $\Delta u = -L_\sigma * di/dt$ induced during di/dt over the parasitic commutation circuit inductance L_σ will increase linear to the decreasing turn-off time.

3.5.3 Driver circuit structures and basic requirements on drivers

Figure 3.40 shows the basic structure of a “comfortable” driver circuit for one MOSFET- or IGBT-bridge arm with TOP/BOTTOM interlock and protection functions close to the gate.
In the depicted driver, TOP and BOTTOM switches and signal processing unit are separated by real potential isolation for control signals, control power and feedback of output and error signals. In “simple” driver circuits these potential isolations may be combined (common energy and signal transmission) or they are partly or even completely omitted (e.g. bootstrap circuits for TOP voltage supply). Low-voltage switches or low-side choppers especially (only BOTTOM switch is active) only require a very simplified driver structure, since single switches can be realized without most interlock and dead-time functions.

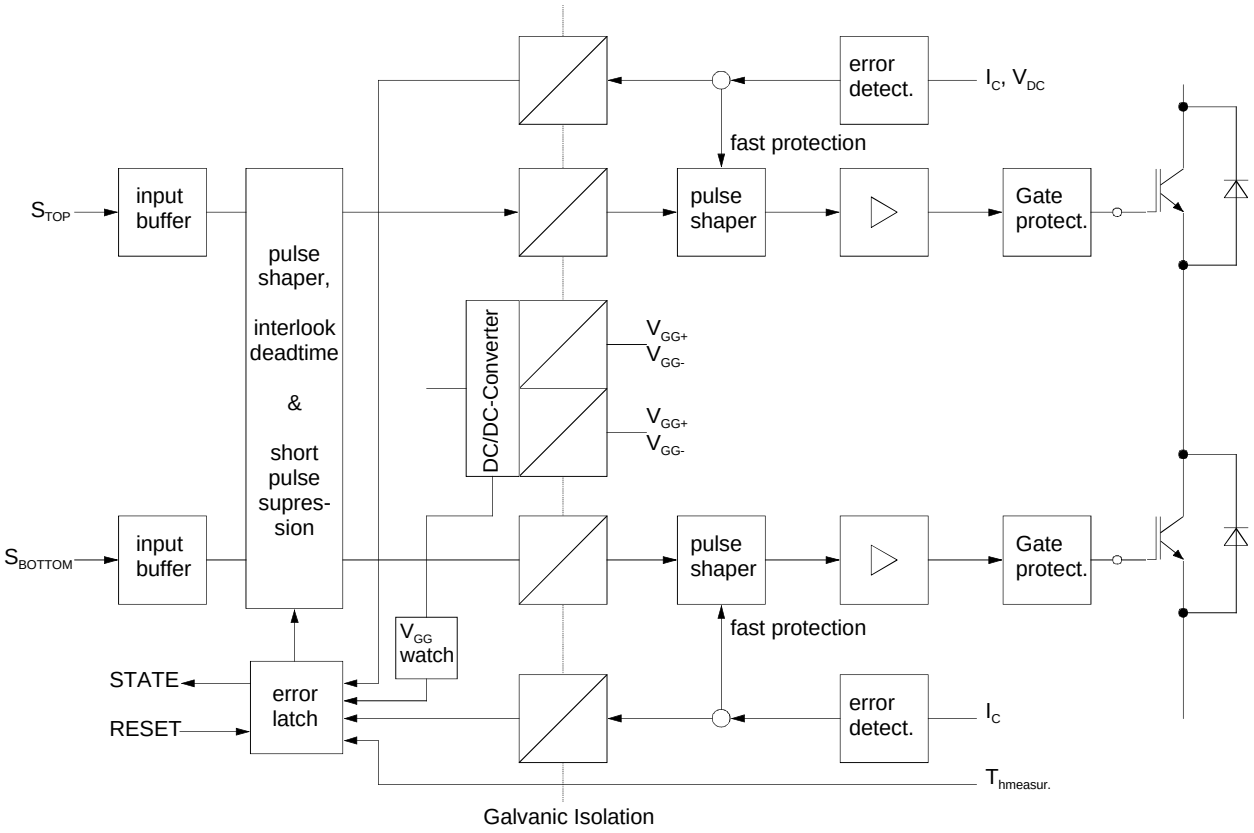


Figure 3.40 Block diagram of bridge arm driver circuit with TOP/BOTTOM interlock and protection (IGBT driver)

The gate unit is the core part of the driver circuit and consists (mostly) of primary-side time control stages for delay, interlock and minimum on and off times (see chapter 3.5.4), potential isolation (with pulse shapers, if necessary) and a generator for positive/negative gate control voltage. The power transistor gate may also be equipped with overvoltage protection, combined with an active clamping for v_{DS} or v_{CE} (see chapter 3.6).

Figure 3.41 shows the principle of a generator for positive and negative gate control voltage (designed for IGBTs with negative gate-emitter voltage).
Apart from the complementary source follower boosters with low-power MOSFETs, for example, complementary drain or collector followers and totem-pole drivers with MOSFETs or bipolar transistors are also commonly used [277].

Further solutions including integrated components are referred to in chapter 3.5.6.

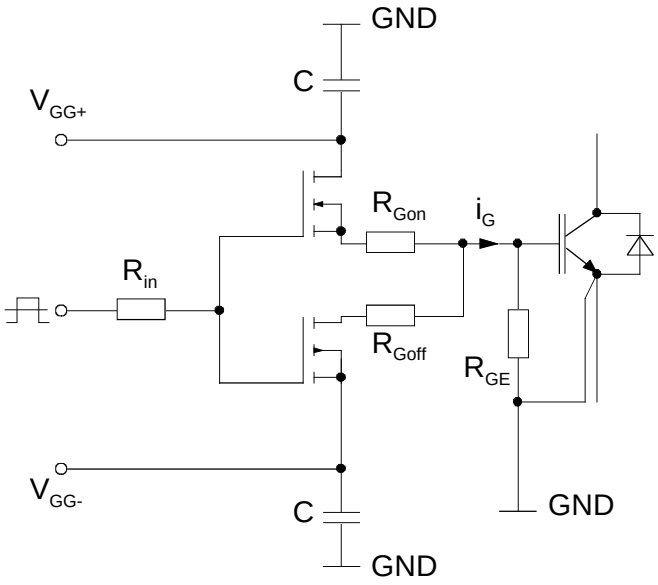


Figure 3.41 Turn-on and turn-off gate voltage generator

The gate resistance R_G in Figure 3.41 has been divided up into two resistors R_{Gon} and R_{Goff} for turn-on and turn-off, respectively. By this means, the mostly inevitable cross current from V_{GG+} to V_{GG-}, generated during switching of the driver MOSFETs, can be limited. The main advantage, however, is that this solution offers the possibility of separate optimization of turn-on and turn-off with regard to turn-on overcurrent and turn-off overvoltage (see chapter 3.5.2) and to short-circuit behaviour (chapter 3.6.2). If only one output is available for R_G, this function can also be maintained by paralleling R_{Gon} and R_{Goff}. Diodes connected in series to the resistors should be arranged so that the cathode is directed towards the IGBT-gate for R_{Gon} and the anode is directed towards the IGBT-gate for R_{Goff}.

The gate-emitter resistor R_{GE} (10... 100 kΩ) should not be omitted in any application, since it prevents unintentional charging of the gate capacitance even under driver operating conditions with highly resistive output levels (switching, off-state and driver supply voltage breakdown).
The low-inductive capacitors C (0.22...1 µF) serve as a buffer for V_{GG+} and V_{GG-} near the driver output and have to keep up a minimum dynamic internal driver resistance together with the low-resistive driver circuit. Only under these circumstances the driver will be able to absorb displacement currents due to dv_{CE}/dt which are conducted via Miller capacitance to the gate and are likely to cause switching failures, parasitic oscillations or inadmissible gate overvoltages.

Moreover, the following aspects have to be considered for the gate voltage generator layout:
- minimum parasitic inductances in the gate circuit, e.g. short (<< 10 cm), twisted connection lines between driver and gate/ driver and emitter; minimum size of circuit arrangement according to Figure 3.41
- elimination of feedback of load current to gate voltage caused by the parasitic emitter inductance in the power module: connection of driver ground to the power module control emitter,
- avoidance of ground loops,
- avoidance of transformative and capacitive coupling between gate and collector circuit (no paralleling of critical tracks or wires; integration of shielded areas).

Of course, these requirements also have to be met by the potential isolated supply of the buffer energy (e.g. by a switch mode power supply integrated in the driver) and by all other functional units on the power transistor potential.
Low-pass filters, pulse shapers and pulse width triggered flip-flops integrated in the signal transmission paths for interference suppression have to live up to the permissible minimum pulse duration and the necessary response times to failures with regard to their delay times.

3.5.4 Integrated protection and monitoring functions of a driver

To protect MOSFET or IGBT modules in case of failure, the implementation of a variety of fast responding and efficient protection functions in the driver is recommended, such as *overcurrent and short-circuit protection*, protection from *excessive drain-source or collector-emitter voltage*, *gate overvoltage protection*, *overtemperature protection* and monitoring of *gate control voltages* V_{GG+} and V_{GG-}.
With reference to Figure 3.40, the integration of protection functions in the driver is explained in the following. Realization and dimensioning aspects are dealt with in chapter 3.6.

Overcurrent and short-circuit protection

The current signal can be generated as an analogous signal (measured via e.g. shunt, current probe, $R_{DS(on)}$ of the driven power MOSFET or sense-source or sense-emitter-cells) or as a maximum rating excess (desaturation of the IGBT). As soon as an error has been detected by comparing the actual value to a fixed maximum rating, an error memory is set (ERROR status) either already on switch potential or - in the case of potential-isolated sensors - in the primary circuit of the driver, which will block the power transistors until the RESET-signal is triggered.
If the error memory is integrated on the secondary side, its state signal will be transmitted to the primary side by a potential-isolated unit. In the case of integration of potential-isolating high-precision current sensors - as for example in SKiiPPACKs and some MiniSKiiP-components - their output signal may serve as actual value for control loops or for detection of ground currents.

Gate-overvoltage-protection

In contrast to all protection functions described so far, the gate protection has to limit periodicly to the gate voltage without detection of an error which would require turn-off of the power transistors. Therefore, there is no connection to the error memory. More details are described in chapters 3.6.1 and 3.6.3.

Protection from excessive drain-source or collector-emittervoltage

Voltage limitation at the main terminals of a power transistor can be realized by the transistor itself (avalanche-proof MOSFETs), by passive networks or by an active circuit, which realizes a defined partial turn-on of the transistor in case of overvoltage (see chapter 3.6.3).
A simple protection, which is not able to detect switching peak voltages and other fast overvoltage peaks, may (option „U“) be optionally integrated into the SKiiPPACK driver as a static DC bus voltage monitoring. A „quasi“ potential isolated sensor will indicate the actual DC bus voltage value and transmits it to the main control circuit as analogous actual value and sets the error memory to ERROR as soon as the limit value has been exceeded. Moreover, a brake chopper buffer may protect for example the DC-link capacitors in case of load energy feedbacks active loads).

Overtemperature protection

The temperature of the power transistor chips and the heatsink temperature near the chips can be determined by the calculation methods described in chapter 3.6.3.3. If the sensor is isolated, the temperature signal (e.g. voltage) may also be transmitted to a main control circuit. A threshold switch on the primary side will set the error memory to ERROR as soon as a limit value has been exceeded.

Supply undervoltage protection of the gate control voltages V_{GG+} and $|V_{GG-}|$.

If the gate control voltage drop considerably, the secondary control, protection and transmission functions may fail. Moreover, the power transistors can no longer be fully controlled or blocked.
In order to detect this critical state in time, either one of the control voltages or the function of the internal power supply of the driver has to be monitored. In case of failure the error memory is set to ERROR.

3.5.5 Time constants and interlock functions

Short-pulse suppression

When pulse transformers or opto-couplers are used for potential isolation of the control signals, the driver has to be especially protected from too low or too short control impulses (interference impulses) which might cause failure of the driver.
Schmitt-triggers, for example, can be connected in series to the potential isolation, which will suppress all turn-on- or turn-off-signals lower than logic level (CMOS, TTL) or < 0.2...0.5 µs. A similar solution may be applied to the secondary side of opto-couplers.

Dead-time for bridge-arm control and arm short-circuit interlock

MOSFETs and IGBTs of the same bridge arm must not be switched on at the same time in voltage source circuits, to avoid a bridge arm short-circuit.
In the static state this may be avoided by interlock of both drivers even if the driver input signals are affected by interferences (not suitable for current source circuits because overlapping operation of the drivers would be required).
Depending on the type of transistor, specific application and driver, the dead time has to total up to t_{dead} = 2...10 µs.

Gating time of a short-circuit protection with measurement of drain or collector current and drain-source or collector-emitter-voltage, respectively

If the transistors are to be turned off because one of the limit values of the given measurement parameters has been exceeded, the turn-on peak current has to be gated from the measurement. When monitoring the desaturation process of an IGBT, the dynamic saturation voltage characteristic has to be considered too. During the first microseconds of the turn-on time $V_{CEsatdyn}$ is considerably increased compared to its final value V_{CEsat} (Figure 3.42). Therefore, the monitoring circuit should respond according to the course of v_{CEsat} during a gating time as indicated in Figure 3.42. For the sake of safe short circuit protection, the gating time is only allowed to amount to 10 µs max. (see chapter 3.6).

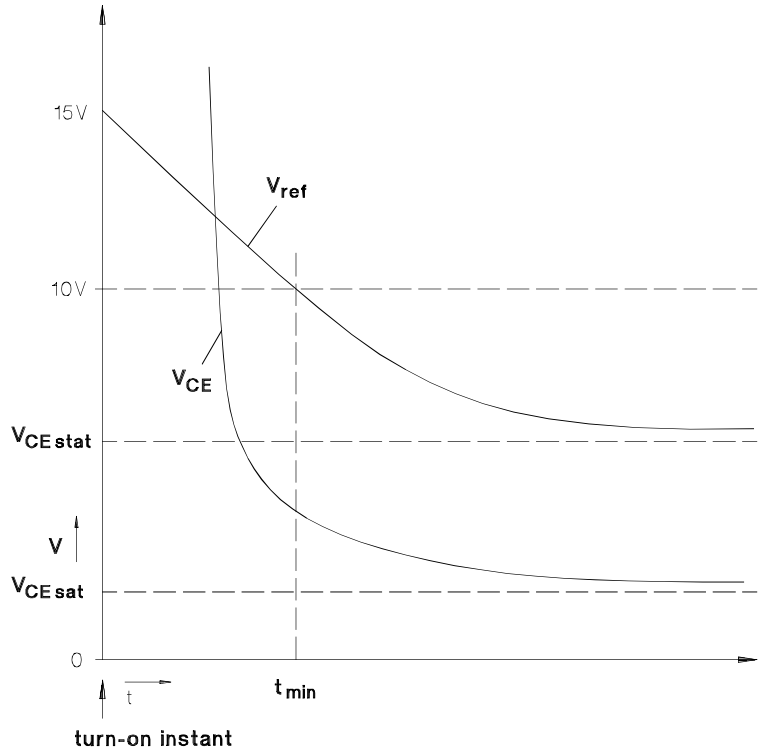


Figure 3.42 Dynamic saturation voltage characteristic of an IGBT and possible protection level V_{ref}

3.5.6 Transmission of control signal and driving energy

ontrol signal and driving energy have to be transmitted from the control unit to the driver stage, which, in return, has to send out state and error signals and, if required, analogous measurement values (current, temperature, DC bus voltage (optional)).

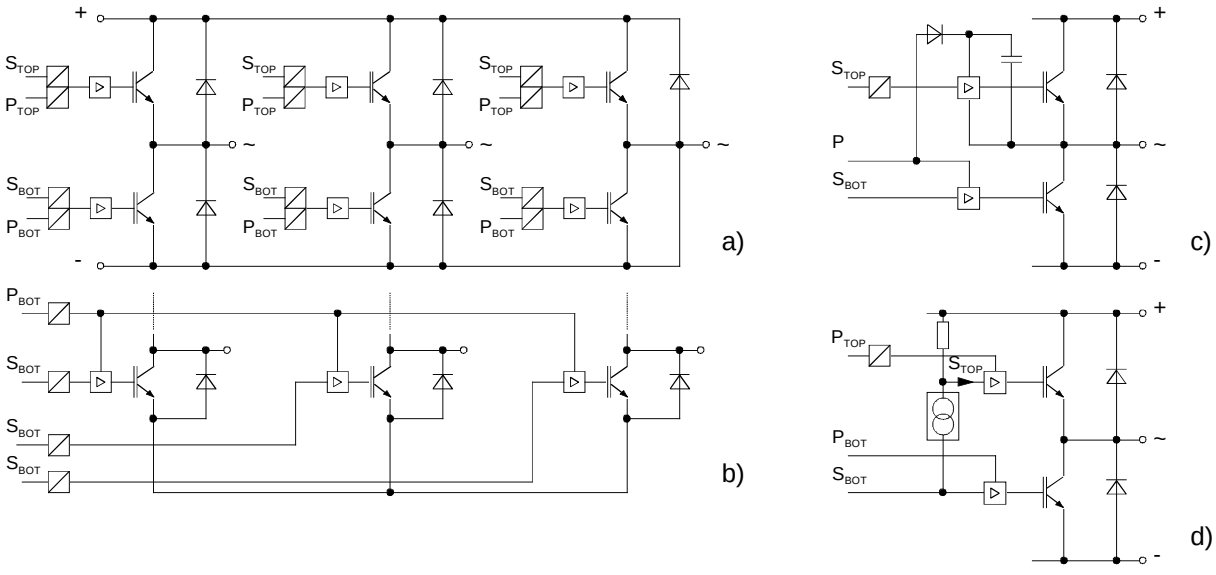


Figure 3.43 Selected signal and energy transmission principles
S_{TOP}, S_{BOT}: control signal for TOP/BOTTOM-switch
P_{TOP}, P_{BOT}: driving energy for TOP/BOTTOM-switch
a) Maximum variant b) Common energy supply of BOTTOM-drivers
c) Bootstrap principle d) Level-shifter principle

In most applications signals are transmitted via optical or transformatory (inductive) potential isolation or via „quasi“ potential isolations, such as bootstrap circuits or level-shifters.
Figure 3.43 shows the scheme of the most important configurations of signal and energy transmission.

Figure 3.43a shows the most common configuration with potential isolations for control signal (S) and driving energy (P), one for each driver circuit. This configuration is preferred (except for low-cost applications) because of its high degree of interference immunity and minimum mutual influence of the switches.
Variant b) contains separate potential isolations for the control signal of all BOTTOM-drivers, but only one common potential isolation for the driving energy of the BOTTOM-drivers .This is used mainly in low-power applications and preferred in many IPMs.
The principle of a bootstrap circuit for energy supply of the TOP-switch without a real potential isolation is depicted in Figure 3.43c. Figure 3.43d shows the scheme of a level-shifter, where the control signal S_{TOP} is transmitted without galvanic isolation via a high-voltage current source.
The simplest solution for applications with very low switching times is to drive the gate directly by means of an pulse transformer, which will transmit the control signal modulated in the driving energy (AC voltage) [277].

The most important requirements to potential isolation are high isolation voltage (2.5...4.5 kV_{eff}) and sufficient dv/dt-ruggedness (15...75 kV/µs).
A high dv/dt-ruggedness can be realized by small coupling capacitances within pF-range from the primary to the secondary side. This will minimize signal transmission interferences caused by displacement currents during switching (Figure 3.44).

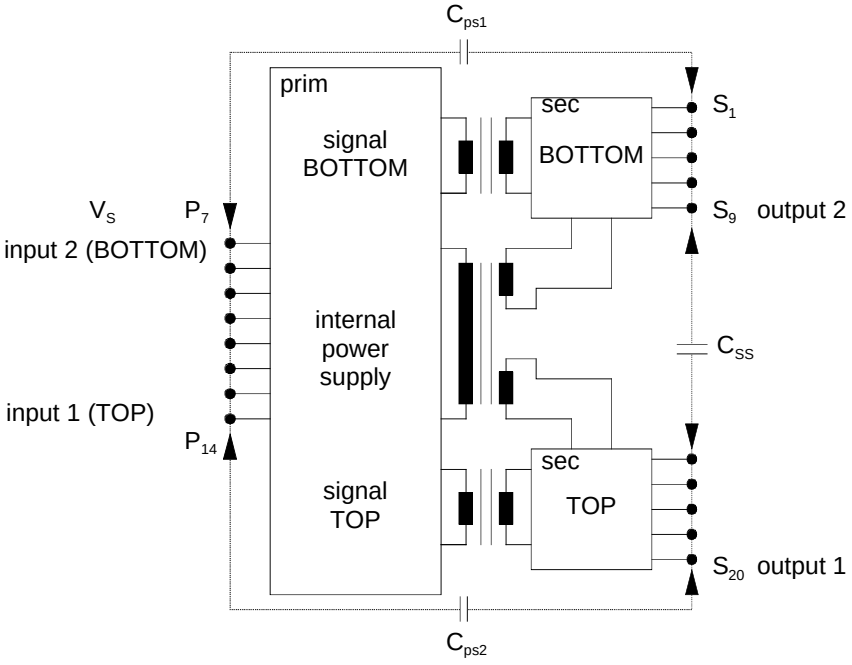


Figure 3.44 Equivalent coupling capacitances in a halfbridge driver with potential isolation
C_{ps1}: Capacitance between primary and TOP-secondary side
C_{ps2}: Capacitance between primary and BOTTOM-secondary side
C_{ss}: Capacitance between secondary side TOP and BOTTOM

3.5.6.1 Control data and feedback

The following table contains the currently most common transmission units with and without potential isolation and their most important features.

Potential isolation	**transformatory**	**optical**	**optical**	**none**
System	Pulse transformer	Opto-coupler	Fiber optic link	Level-shifter
for power modules up to	> 1700 V	1700 V	> 1700 V	1200 V
Transmission directions	bi-directional	uni-directional	uni-/bi-directional	uni-directional
Duty cycle restriction	yes	no	no	no
Coupling capacitance	5...20 pF	1...5 pF	< 1 pF	> 20 pF
dv/dt-immunity	high	low	high	low
Costs	medium	low	high	low

Supported by additional circuitry, pulse transformers are able to transmit feedback signals as state informations during break times of the driver (e.g. dead time in halfbridge circuits); fiber optic links equipped with double transmitters / receivers will work the same way.
Analogous output signals may be fed back from the driver to the main control unit for example in a pulse-width modulated state by additional pulse transformers, opto-couplers or fiber optic links.
The potential isolation is already integrated in current probes with Hall-sensors or compensated magnetic sensors.

3.5.6.2 Driving energy

The basic, currently applied solutions and their most important features are mentioned in the following:

Potential isolation	**transformatory**			**none**
System	50 Hz-power supply	Switch-mode power supply		Bootstrap-circuit
Supplied by	Auxiliary voltage or mains voltage	Auxiliary voltage	DC-link	Operating voltage on BOTTOM-side
AC-frequency **smoothing requirements**	low high	very high very low	medium low	medium (pulse fr.) low
for power modules	1200 V	>1700 V	1700 V	1200 V

Output voltage	positive and negative	positive and negative		only positive
Duty cycle restriction	no	no	no	yes
Coupling capacitance	high	low	medium	low
Interference emission (HF)	none	high	low	none
Costs	low	low	high	very low

3.5.7 Driver circuits for power MOSFETs and IGBTs

In most cases, modern drivers are equipped with monolithical driver ICs which are available as single, half-bridge and full-bridge drivers in a large variety.
The function spectrum of these circuits mostly comprises:

- gate voltage generator;
- input for V_{CEsat}- or $V_{DS(on)}$-monitoring, sometimes also input for shunt or sense-emitter;
- supply undervoltage monitoring;
- error memory and error feedback output ;
- adjustable dead time generation and bootstrap power supply of the TOP-driver.

These standard drivers do not provide a real potential isolation. For some variants, the control input may be configured for connection of opto-couplers or pulse transformers.

Moreover, progress is being made in the development of fast opto-couplers with power driver output which have already integrate supply undervoltage- and V_{CEsat}- or $V_{DS(on)}$-monitoring. To achieve simple driver units, a DC/DC-converter and few passive components merely have to be added.

With the growing variety of function and protection parameters in driver circuits, the assemblies necessary on the primary side also have to live up to more sophisticated requirements comprising, for example, input signal logic, short-pulse suppression, dead time generation, error memory and error evaluation, control of the DC/DC-converter and drive of the pulse transformers.

For the production of low-cost driver circuits, these functions have been combined in a control-ASIC developed by SEMIKRON called SKIC 2001 [154]. The SKIC 2001 is applied in SEMIKRON drivers and is also available as a single IC.

3.5.8 SEMIDRIVER

SEMIDRIVERs are driver components for IGBT and MOSFET power modules (single switches, bridge arms or 3-phase inverters) integrating mainly those function parameters depicted in the block diagram of Figure 3.40. They are being produced in different types either as SKiiPPACK-drivers or OEM-drivers for IGBT and MOSFET power modules.

3.5.8.1 OEM-drivers [225], [264], [272]

The following table shows a survey on the most important OEM-SEMIDRIVERs and their main features.

SKHI	10, 10/17	21A,	22A,B 22A,BH 4	23/12, 23/17	24	26W, 26F	27W, 27F	61 71	BS01, BS02	SKAI 100
Driver	A	B	B	B	B	B	B	D/DL	DL	L
Type	PCB	Hybr.	Hybr.	PCB	Hybr.	PCB	PCB	Hybr.	Subpr.	PCB
V_{iso}/kV, AC1min	4	2.5	2.5 4	4	4	2.5	4	2.5	2.5	2.5
Signal trans-mission	I (FO)	I	I	I (FO)	I	I FO	I FO	OC	OC	OC
V_{GG+}/V	15	15	15	15	15	15	15	15	15	15
V_{GG-}/V	-8	0	-8	-8	-8	-8	-8	-6.5	-8	0
I_{GAV}/mA	100	40	40	50	80	100	150	20	15	90
I_{GM}/A	8	8	8	8	1.5	8	30	2	1	1.5
dv/dt/ kV/µs	75	50	50	75	50	75	50	15	15	50
V_{CEsat}-monitoring for V_{CE}/V	600 1200 1700	600 1200	600 1200 1700	600 1200 1700	600 1200 1700	600 1200	600 1200 (1700)	600 1200	- -	600 1200 1700
Short-circuit soft turn-off	+	-	-	+	-	+	+	+	-	-

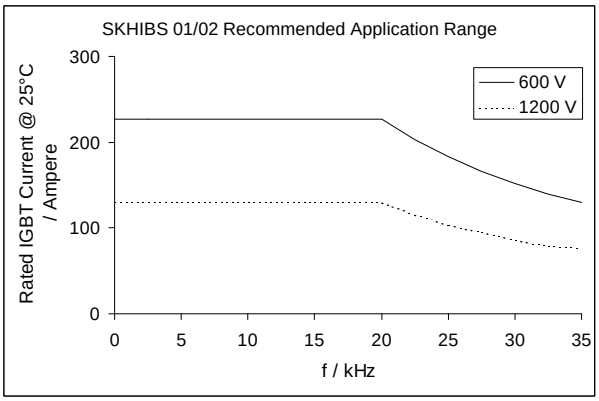
A: Single driver
B: Bridge arm driver (Dual)
I: Pulse transformer
FO: Fiber optic link
OC: Opto-coupler
D: Driver for three-phase inverter
L: Driver for brake chopper
DL: Driver for three-phase inverter and brake chopper
(): Interface optional
*: TOP-switch (BOTTOM-switch: 10kV/µs)

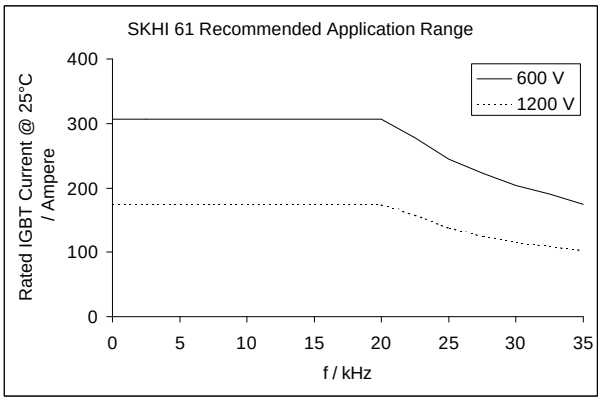
Features valid for all SEMIDRIVERs are:

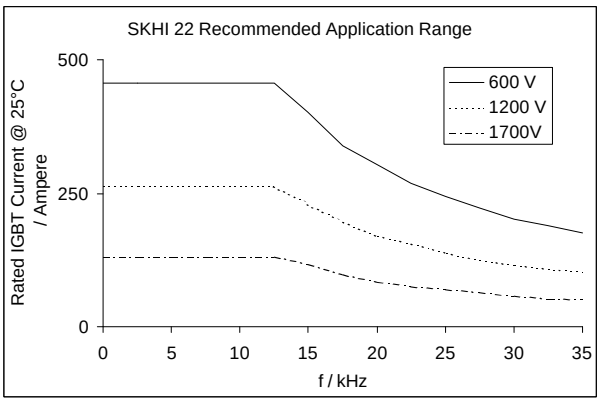
- Power supply +15 V on information potential (SKAI 100 also 24 V); integrated SMPS with potential isolation,
- 15 V-C-MOS and/or 5 V TTL-compatible inputs with potential isolation using pulse transformers or opto couplers,
- Short-circuit protection via V_{CE} or current sensor inputs (SKHIBS 01/02),
- Supply undervoltage monitoring < 13 V,
- Error memory and error feedback output,
- Variable dead time between driver TOP and BOTTOM for bridge arms,
- Short-pulse suppression.

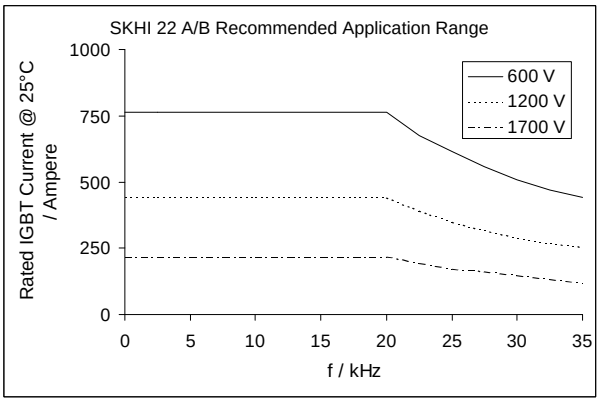
For the SKHI 24 and SKHI 22B it is possible to cancel the dead time between TOP and BOTTOM and, thus to drive the TOP and BOTTOM switch synchrounously or in overlap mode (e.g. CSI topologies).

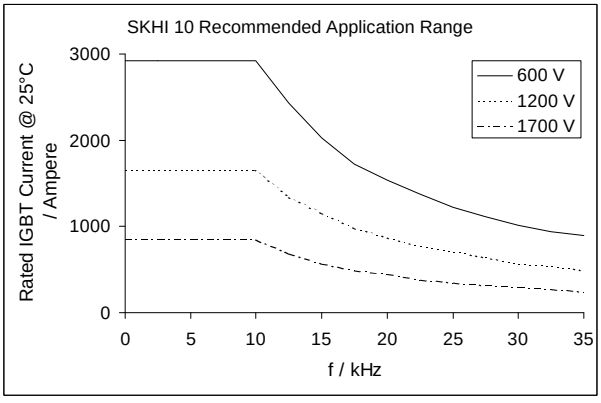
Figure 3.45 illustrates which IGBTs of the SEMITRANS product range may be driven up to which switching frequency by the drivers mentioned on the top of each diagram. For this, the rated IGBT current I_C@25°C has been plotted in the ordinates. The diagrams are valid for SEMIKRON modules with the voltage grade designations and series numbers 063 (600 V), 123 (1200 V) and 173 (1700 V). For other IGBT modules the values have to be adapted to the input capacitances of the IGBTs which may vary from generation to generation.

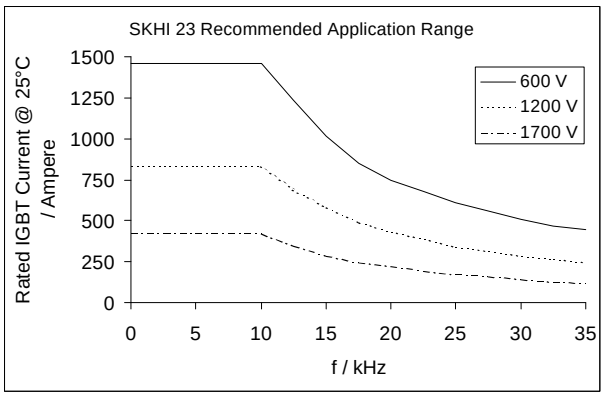

SKHIBS 01/02 Recommended Application Range
Rated IGBT Current @ 25°C / Ampere
f / kHz
600 V
1200 V

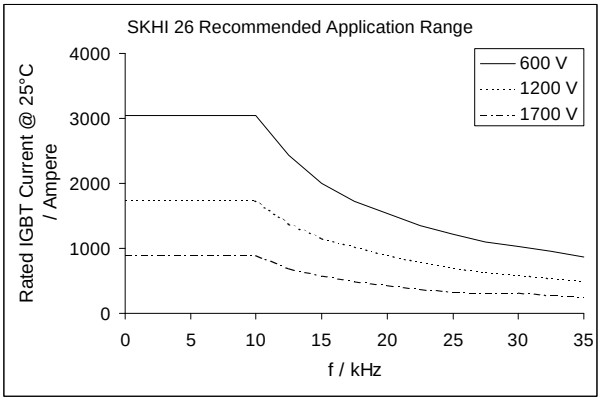

SKHI 61 Recommended Application Range
Rated IGBT Current @ 25°C / Ampere
f / kHz
600 V
1200 V

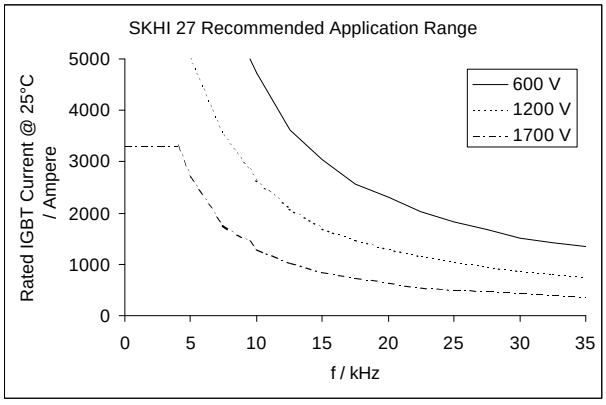

SKHI 22 Recommended Application Range
Rated IGBT Current @ 25°C / Ampere
f / kHz
600 V
1200 V
1700V


SKHI 22 A/B Recommended Application Range
Rated IGBT Current @ 25°C / Ampere
f / kHz
600 V
1200 V
1700 V


SKHI 10 Recommended Application Range
Rated IGBT Current @ 25°C / Ampere
f / kHz
600 V
1200 V
1700 V


SKHI 23 Recommended Application Range
Rated IGBT Current @ 25°C / Ampere
f / kHz
600 V
1200 V
1700 V


SKHI 26 Recommended Application Range
Rated IGBT Current @ 25°C / Ampere
f / kHz
600 V
1200 V
1700 V


SKHI 27 Recommended Application Range
Rated IGBT Current @ 25°C / Ampere
f / kHz
600 V
1200 V
1700 V

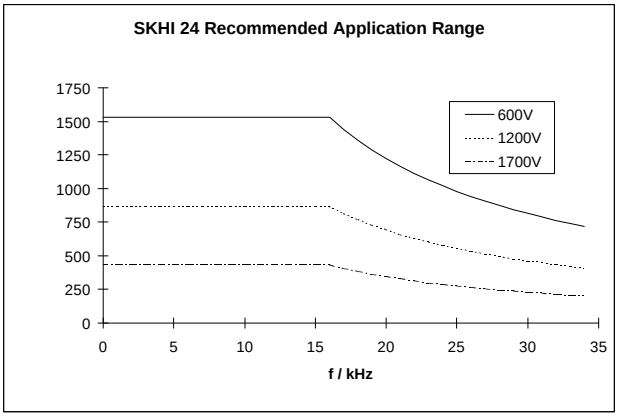


Figure 3.45 IGBT current and switching frequency ranges of SEMIDRIVERs

3.5.8.2 SKiiPPACK-drivers [112], [264]

All SKiiPPACK drivers mentioned in chapter 1.5.1 and 1.6 have been optimized with regard to IGBT chips and inductances within the SKiiPPACKs, which guarantees optimal utilization of chips, high interference immunity and a high degree of failure protection.
As an example, Figure 3.46 shows the block diagram of a SKiiPPACK dual module GB-driver.

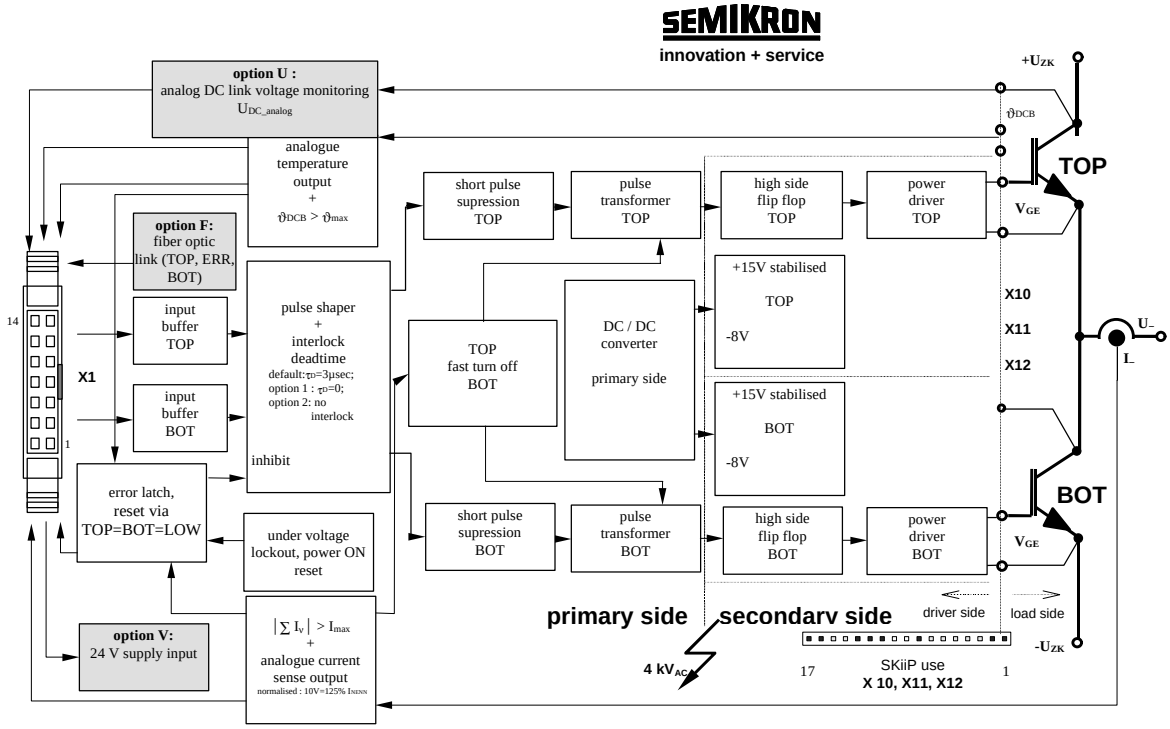


Figure 3.46 Block diagram of a GB-driver for a SKiiPPACK dual module

Basic features of SKiiPPACK-drivers:

- + 24 V supply voltage uncontrolled or + 15 V $\pm$ 4 % on information potential; integrated SMPS with potential isolation;
- 15 V CMOS input signal level; pulse transformers
- Isolation voltage (AC, 1 min) primary/secondary 3 kV_{eff} for SKiiPPACK 600 V, 1200 V, 4 kV_{eff} for SKiiPPACK 1700 V (3,5 kV_{eff} for GDL-brake chopper);
- dv/dt-ruggedness min 75 kV/µs (50 kV/µs for GDL-brake chopper)
- Error memory with error feedback output (open-collector-output)

- Optional fiber optic input (option F);
- Current sensors, overcurrent/short-circuit protection by potential isolating current sensors in the AC-outputs (for H-bridges and three-phase-bridges ground current monitoring at the same time);
- Heatsink temperature sensors and monitors (near the chips);
- Supply undervoltage monitoring of the driver supply voltage;
- Optional DC-link voltage monitoring (option U).

For interlocking, input short-pulse suppression (<750 ns), dead time generation and interlock TOP/BOTTOM have been implemented.

Current sensing and overcurrent protection

Figure 3.47 explains the principle of analogous current measurement via current sensors integrated close to the AC-terminals in the SKiiPPACK case frame.

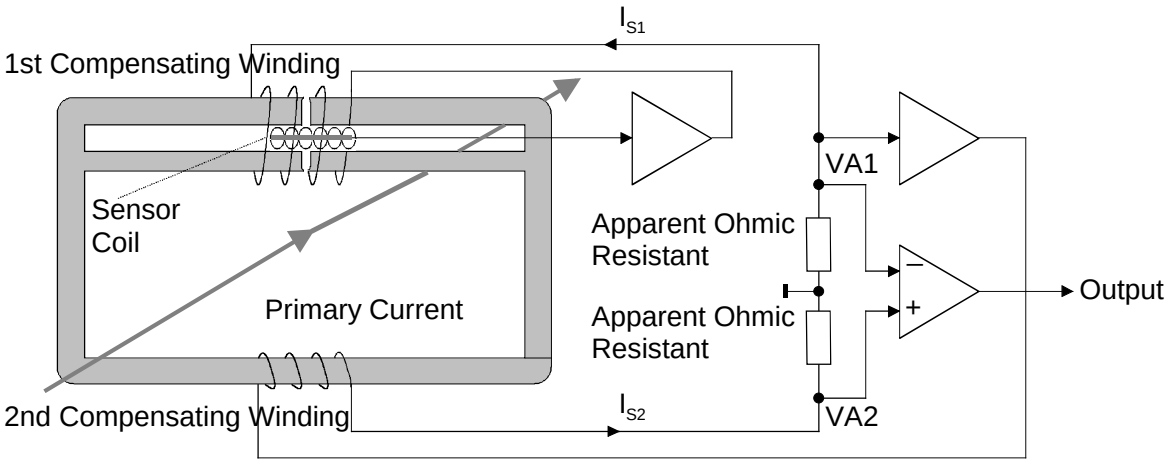


Figure 3.47 Principle of current sensors integrated in SKiiPPACK and MiniSKiiP 8..I

The AC-output current of each phase is transmitted inductively into a magnetic field sensor, which will detect positive and negative magnetic field peaks. The sensor current is controllable via compensation windings, by which the output current will be reflected.
This method may even be used in power module applications subject to high thermal stress, because no offset due to temperature will be generated in contrast to Hall-sensors. The sensor is characterized by a small measuring fault (< 0,25 %), a low degree of non-linearity (< 0.1 %) and short response times (< 1 µs). Direct and alternating current may be measured, respectively.
The output currents of SKiiPPACK driver sensors have been summarized and normalized in such a way that the type current (I_C@25°C) indicated in the datasheets will generate a voltage of 8V at the actual current output of the SKiiPPACK. The direction of voltage corresponds to the direction of AC-current flow (> 0 V: current flow out of the SKiiPPACK/< 0 V: current flow into the SKiiPPACK).
As soon as 125 % of I_C@25°C has been reached, this voltage will increase to its limit value of 10V, and the OCP inside the SKiiPPACK will be triggered off (OCP: **O**ver **C**urrent **P**rotection). The IGBTs will be turned off within 1 µs and the error memory will be set.

Figure 3.48 explains the advantages of OCP compared to overcurrent protection by V_{CE}-monitoring.

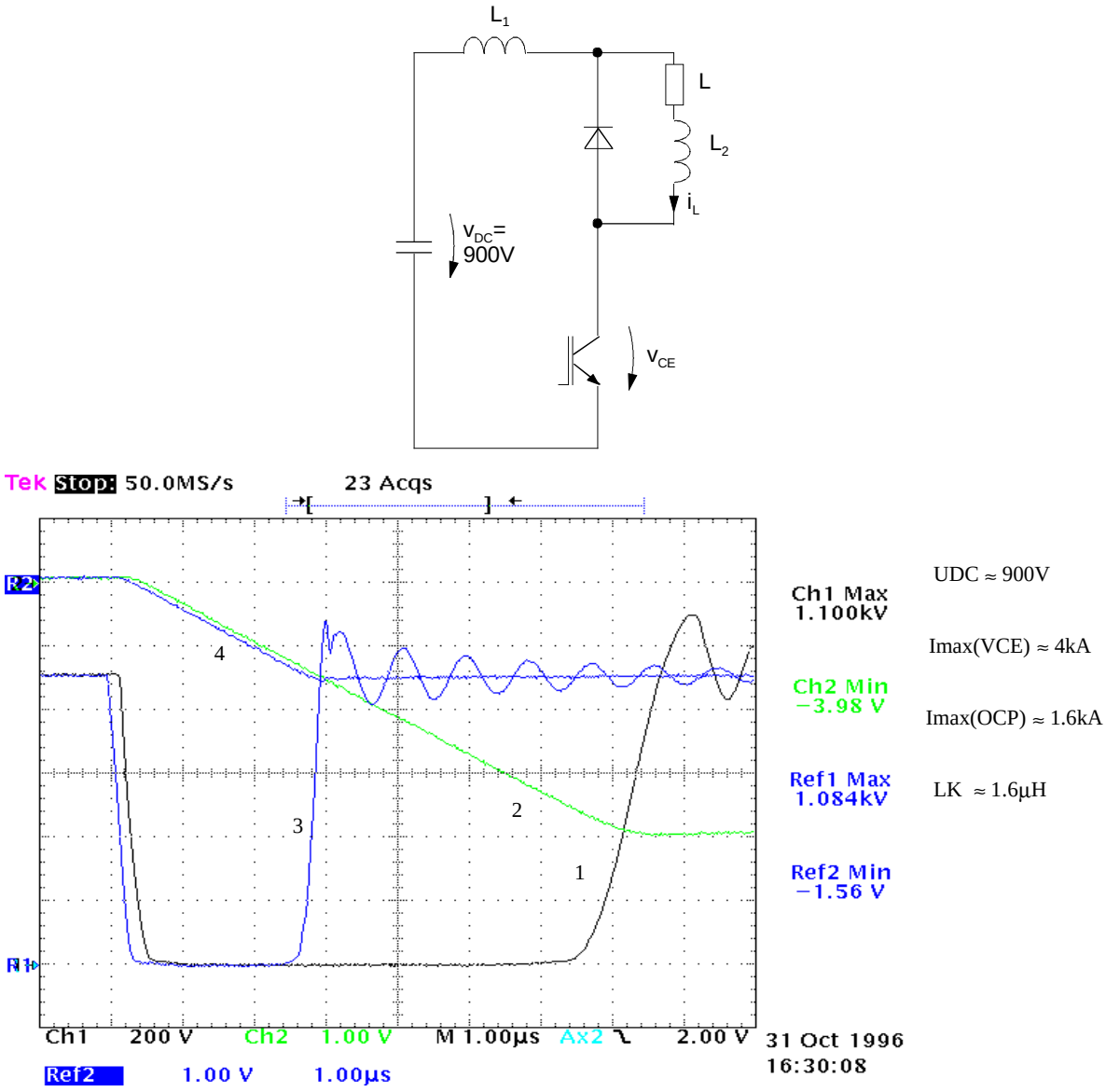


Figure 3.48 Current and voltage characteristics during overcurrent case I for V_{CE}-monitoring and OCP
1) v_{CE}-characteristic at overcurrent turn-off by v_{CE}-monitoring
2) i_L-characteristic (inverted) at overcurrent turn-off by v_{CE}-monitoring
3) v_{CE}-characteristic at overcurrent turn-off by OCP
4) i_L-characteristic (inverted) at overcurrent turn-off by OCP

With the OCP-principle overcurrents will be detected and turned off earlier than with V_{CE}-monitoring, since no gating time comparable to V_{CE}-monitoring will be required. Moreover, the turn-off threshold level is not dependent on the temperature as with V_{CE}-protection, where, for example, $I_{CERROR} = 1.25I_C$@25°C is set for $V_{CEERROR}$@125°C. Due to the positive temperature coefficient of the saturation voltage in NPT-IGBTs, a considerable higher collector current might flow on reaching the switching threshold $V_{CEERROR}$@125°C in a cold IGBT (about doubled at 25°C/tripled at -25°C).
The high collector current may possibly result in a high turn-off overvoltage.
The ability of modern IGBTs to turn off very fast in a wide range of the gate control (gate resistance R_{Goff}), however, may cause high turn-off overvoltages even during short-circuit soft turn-off, which in most cases requires I_C deratings.

Temperature sensing/ overtemperature protection

Temperature sensing is managed by a PTC-resistor with almost linear characteristic, which is arranged on the DCB-substrate of one phase. The output signal is amplified and is provided as a normalized analogous signal with a maximum error of 5 % within the range of 40...125°C and is used for overtemperature turn-off at 115°C ± 3 K.
The analogous signal is normalized to 2 V at 41.5°C and 10 V at 117.5°C.

DC-link voltage detection (option U)

The DC-link voltage is detected by a highly resistive differential amplifier input which meets the requirements of standard VDE 0160/EN 50178 (safe electrical isolation).
The output signal is normalized to 9 V corresponding to voltage V_{dmax} (measurement error 2 %).

Aquisition and evaluation of analogous signals

Thanks to the thoroughly EMI-conforming driver concept, shielded cables can mostly be done without, even if long wires are used.
To guarantee faultless processing of the analogous SKiiPPACK signals, however, it is important to avoid ground loops and voltage drops in measuring wires which are not caused by measuring signals. Therefore, measuring currents have to be conducted on the ground side via the AUX-GND-connections and not via power supply ground lines (see Figure 3.49).

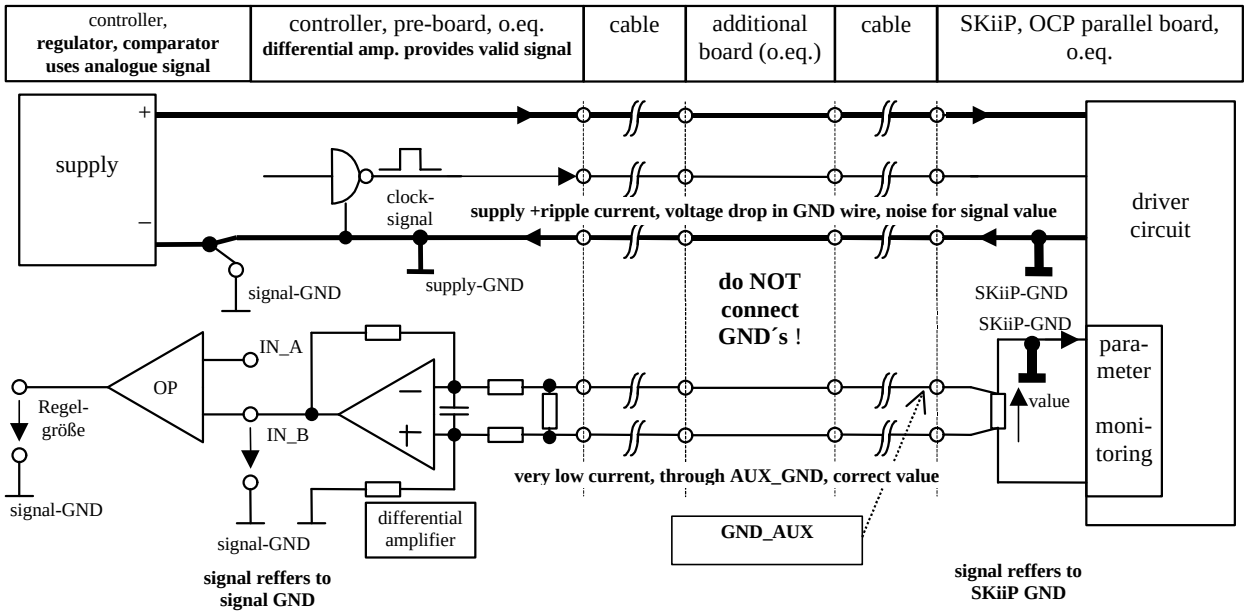


Figure 3.49 Processing of analogous SKiiPPACK output signals

In the case of interferences in the environment we recommend the evaluation of any analogous signal via a differential amplifier with reference to auxiliary ground (SEMIKRON: AUX-GND). Remaining interference spikes should be filtered out by low-pass filters.

Further application hints with regard to SKiiPPACK-drivers are given in the SEMIKRON databook [264].

Test equipment for batch production of SKiiPPACKs ▷

3.6 Fault behaviour and protection

3.6.1 Types of faults

Components used in power electronics have to be protected from non-permissible stress in any operational state - i.e. they have to be protected from leaving the safe operation areas indicated in the datasheets.
Leaving SOAs will cause damage and, therefore, reduce component life. In the worst case, the component might be destroyed immediately.
Therefore, it is most important to detect critical states and faults first, and to respond to them adequately afterwards.
The explanations in this chapter refer mainly to IGBTs, but may be applied to power MOSFETs in analogy. Special notes with regard to MOSFETs are indicated separately.

Fault currents

Fault currents are collector-/drain currents, which exceed standard operating values of a certain application due to control or load errors.
They might lead to damage of the power semiconductors by the following mechanisms:
- thermal destruction by high power dissipation,
- dynamic avalanche,
- static or dynamic latch-up,
- overvoltages due to fault currents.

A difference is made between the following fault currents:

Overcurrent

Features:
- low collector current di/dt (depending on load inductance and driving voltage),
- fault current is conducted through the DC-link,
- transistor does not desaturate,

Causes:
- reduced load impedance,
- inverter control error,

Short-circuit current

Features:
- very steep collector current di/dt,
- fault current is conducted through the DC-link,
- transistor is desaturated,

Causes:
- Arm short-circuit (case 1 in Figure 3.50)
  + by defective switch
  + by faulty driver pulses for the arm switches
- Load short circuit (case 2 in Figure 3.50)
  + by faulty isolation
  + “man-made” errors (wrong connection wiring etc.)

Earth fault current (case 3 in Figure 3.50)

Features:
- Collector current di/dt is dependent on earth inductance and driving voltage
- Earth fault circuit is not closed over DC-link
- Desaturation of the transistor is dependent on fault current value

Causes:
- Connection between a voltage-carrying conductor and earth potential (by faulty isolation or „man-made“ errors)

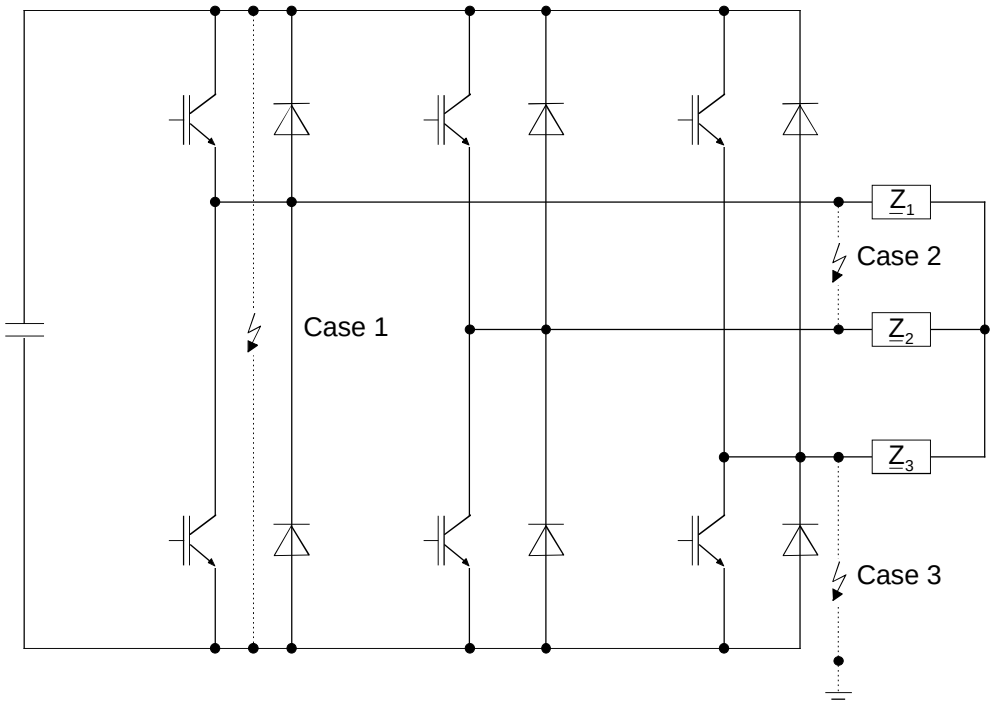


Figure 3.50 Causes of fault currents

Overvoltages

We are talking about dangerous overvoltages, if the avalanche break-down voltages of power semiconductors are exceeded. This goes for transistors as well as for diodes.
With respect to IGBTs and MOSFETs, overvoltages may occur between collector and emitter (or drain and source) - i.e. between the main terminals - as well as between gate and emitter (or gate and source) - i.e. between the control terminals.

Causes of overvoltages between main terminals:

Figure 3.51 shows different types of overvoltages between main terminals of power semiconductors with the example of a commutation circuit.

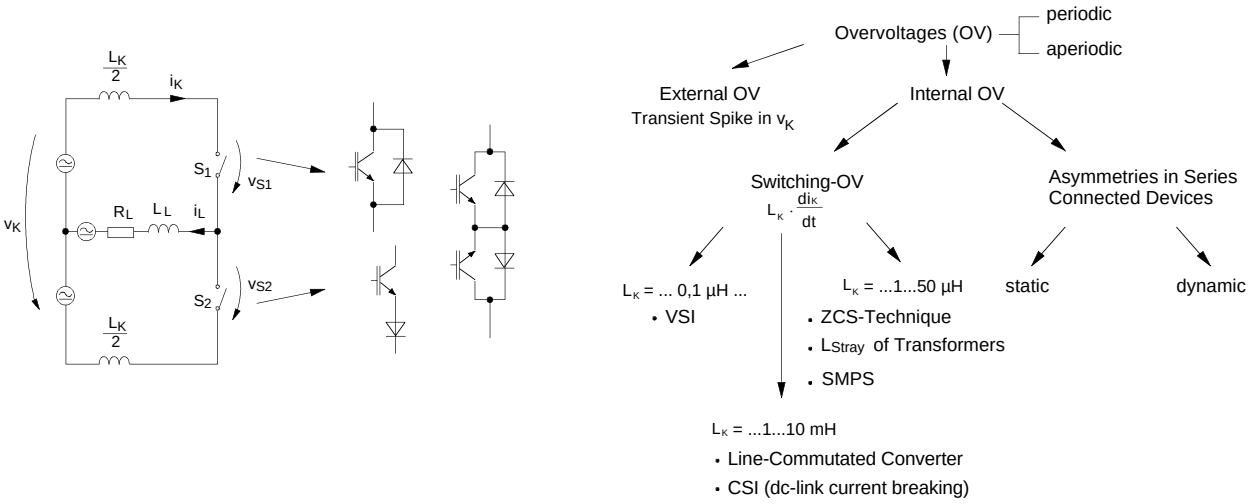


Figure 3.51 Types of overvoltages

Overvoltages in a commutation circuit may principally be divided into external and internal overvoltages.
In this respect, an „external overvoltage“ is to be comprehended as transient increase of the impressed commutation voltage v_K. This may happen for example in DC-voltage mains of electric traction. Increased DC-link voltages are to be regarded in the same manner (caused e.g. by active feedback loads or control errors in pulse rectifiers).
“Internal overvoltages” are generated by turning off the power-electronic switch against the commutation circuit inductance L_K ($\Delta v = L_K * di_K/dt$).
The following processes are characteristic for the generation of switching overvoltages:

- Active turn-off of load current i_L by the active elements of switches S_1 and S_2 during normal operation of a converter:
  In many SMPS-applications (Switch-Mode Power Supply) the inductance L_K is due to the stray inductance of transformers, which may amount up to 10-100 µH.
- Reverse-recovery-di/dt during passive turn-off (reverse recovery) of fast diodes in hard switching converters or ZCS-converters:
  due to their operation principle, ZCS-converters may also show an increased commutation inductance within the range of 10 µH (see chapter 3.8).
- High di/dt (...10 kA/µs...) in case of short circuits and during turn-off of short circuit currents in converters with DC voltage link ,
- Active interruption of DC link currents in CSI-topologies (big inductances).

Furthermore, overvoltages in power electronic devices may be generated by static or dynamic asymmetries of switches connected in series (see chapter 3.7).

Overvoltages during normal operation of converters and converter fault operation may appear as periodic (...Hz...kHz...) or aperiodic overvoltages

Causes of overvoltages between control terminals:

Overvoltages between control terminals of IGBTs and MOSFETs can be due to:
- supply voltage error of the driver,
- dv/dt-feedback (displacement current to the gate) via Miller capacitance (e.g. short circuit II, see chapter 3.6.2),

- emitter-/source-di/dt-feedback (see chapter 3.4.1),
- increase of gate voltage during active clamping (see chapter 3.6.3.2).

Overtemperature

Dangerous overtemperatures arise, if the maximum junction temperature indicated by the device manufacturer is exceeded (e.g. T_{jmax} = 150°C for silicon devices).

During inverter operation overtemperatures might be generated by:
- increase of energy dissipation caused by fault currents,
- increase of energy dissipation caused by defective drivers,
- failure of the cooling system.

3.6.2 Behaviour of IGBTs and MOSFETs during overload and short-circuit operation

Overload:

Basically, the switching and on-state behaviour under overload does not distinguish from „standard operation“ under rating conditions. In order not to exceed the maximum junction temperature, the overload range has to be restricted, since increased load current will cause increased power dissipation in the device.
In this respect limits are set by the absolute value of the junction temperature as well as by overload temperature cycles.
These limits are indicated in the datasheet SOA-diagrams.
Figure 3.52 shows selected examples for MOSFETs and IGBTs.

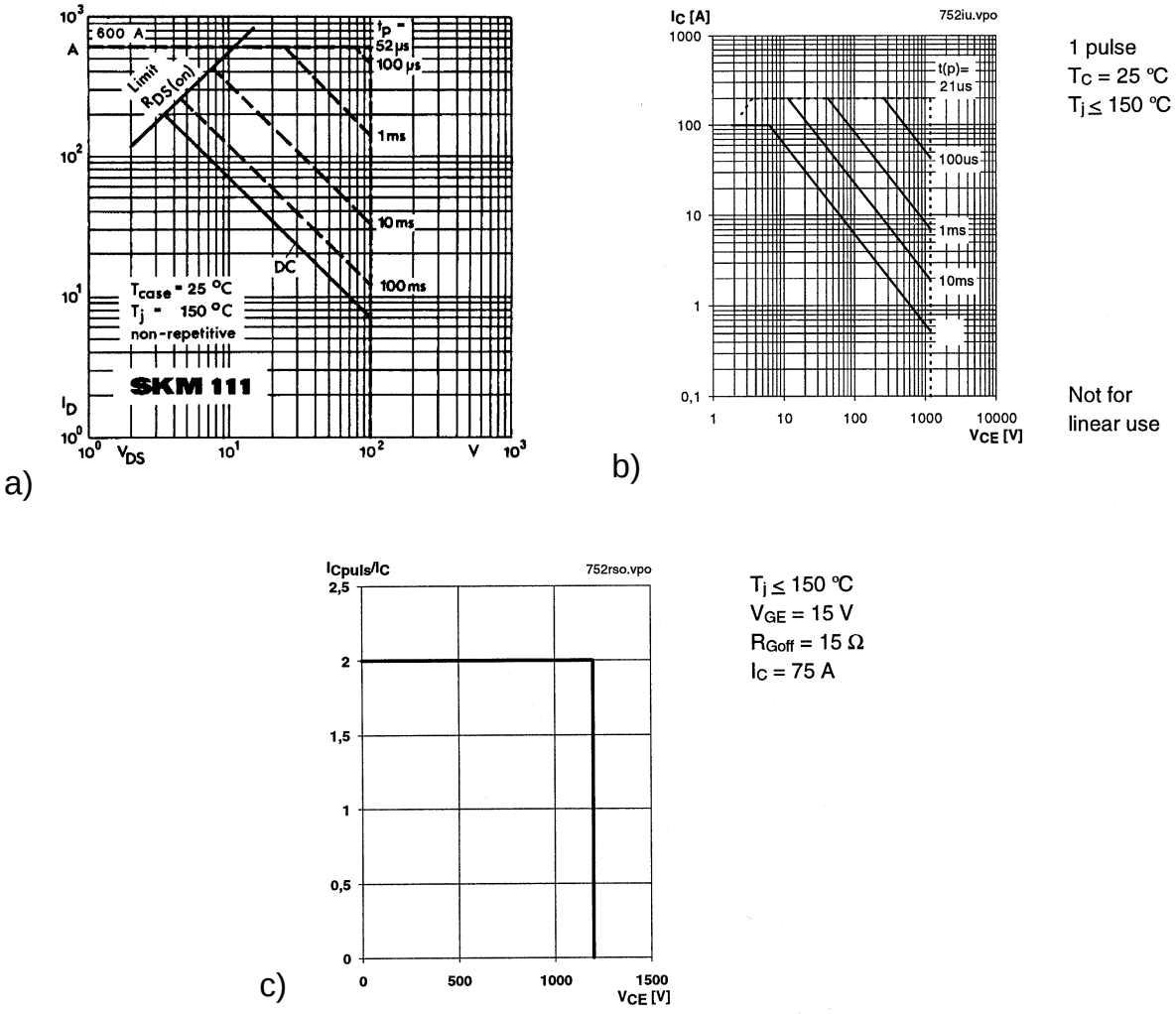


Figure 3.52 SOA-diagrams for MOSFETs and IGBTs
a) Max. safe operating area MOSFET SKM111
b) Max. safe operating area IGBT SKM100GB123D
c) Turn-off safe operating area (! periodic !) IGBT SKM100GB123D

Short circuit:

Principally, IGBTs and MOSFETs are short-circuit proof, i.e. they may be subjected to short circuits under certain given conditions and turn them off, without damaging the power semiconductors.

When considering short circuits (which is to be done with IGBTs), two different cases of short circuits have to be distinguish.

Short circuit I (SC I)

In case of SC I the transistor is turned on to an existing load short circuit, i.e. full DC-link voltage is applied to the transistor already before the short circuit occurs. The di/dt of the short-circuit current is determined by the driver parameters (driver voltage, gate resistor). This transistor current increase will induce a voltage drop over the parasitic inductance of the short circuit, which is depicted as a decrease of the collector-emitter voltage characteristic (Figure 3.53).

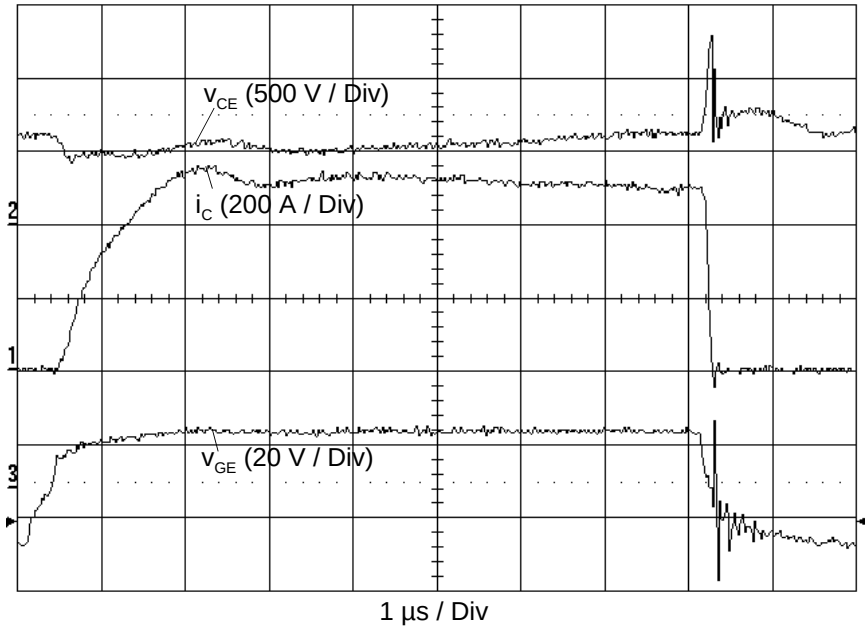


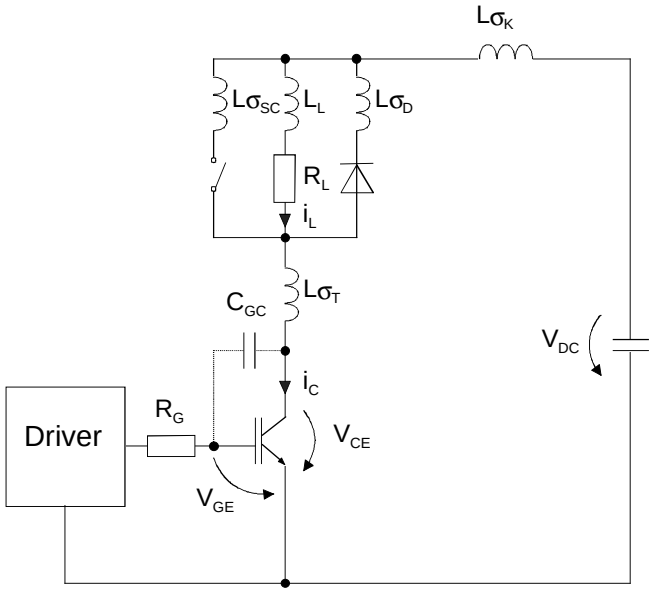
Figure 3.53 SC I characteristics of an IGBT (SKM100GB123D)

The stationary short-circuit current adjusts itself to a value that is determined by the output characteristic of the transistor. Typical values for IGBTs are up to 8-10 fold rated current (see Figure 3.56b).

Short circuit II (SC II)

In this case the transistor is already turned on, before the short circuit occurs. Compared to SC I, this case is much more critical with respect to transistor stress.

Figure 3.54 shows an equivalent circuit and principle characteristics to explain the SC II process.



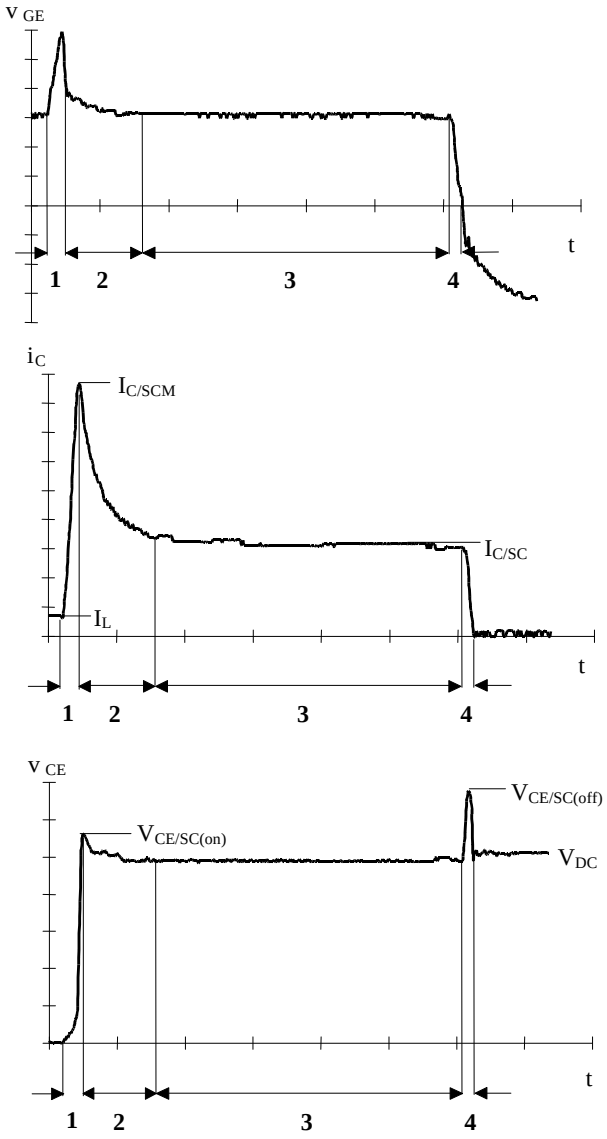


Figure 3.54 Equivalent circuit and principle characteristics of SC II [194]

As soon as the short circuit has occurred, the collector current will increase very steeply, the di/dt is determined by DC-link voltage V_{DC} and the inductance of the short-circuit loop.

During time interval 1 the IGBT is desaturated. The consequently high dv/dt of the collector-emitter voltage will effect a displacement current through the gate-collector capacitance, which increases the gate-emitter voltage. This in turn will cause a dynamic short-circuit peak current $I_{C/SCM}$.

After having completed the desaturation phase, the short-circuit current will drop to its static value $I_{C/SC}$ (time interval 2). During this procedure, a voltage will be induced over the parasitic inductances, which becomes effective as overvoltage in the IGBT.

The stationary short-circuit phase (time interval 3) is followed by turn-off of the short-circuit current towards the commutation circuit inductance L_K, which will again induce an overvoltage to the IGBT (time interval 4).

The transistor overvoltages induced during a short circuit may exceed the values of normal operation by several times.

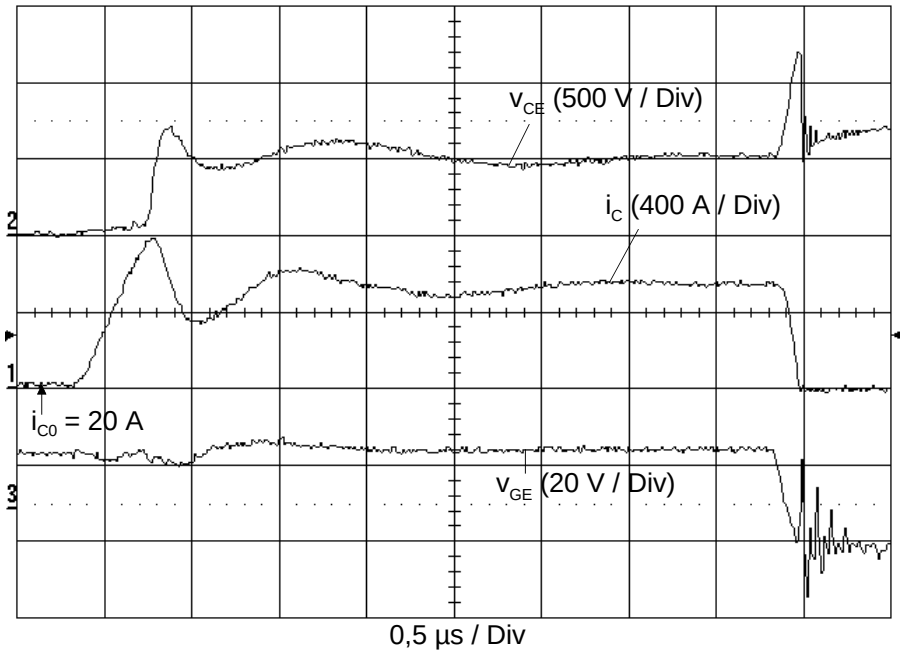
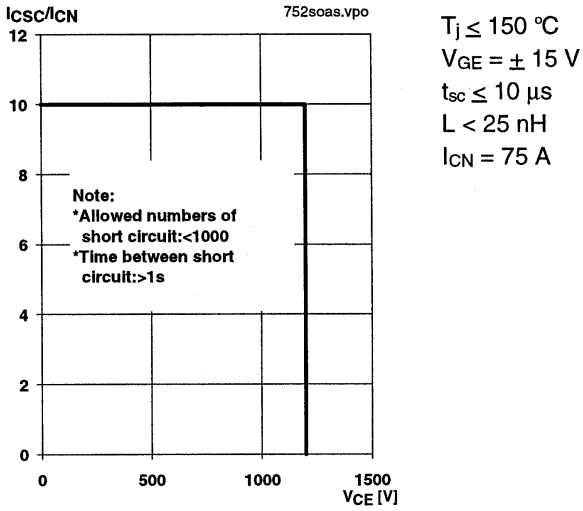


Figure 3.55 SC II characteristics of an IGBT (SKM100GB123D with gate clamping)

The SOA-diagram at short circuit shown in the IGBT datasheets shows the limits for safe control of a short circuit (Figure 3.56a).

a)



b)

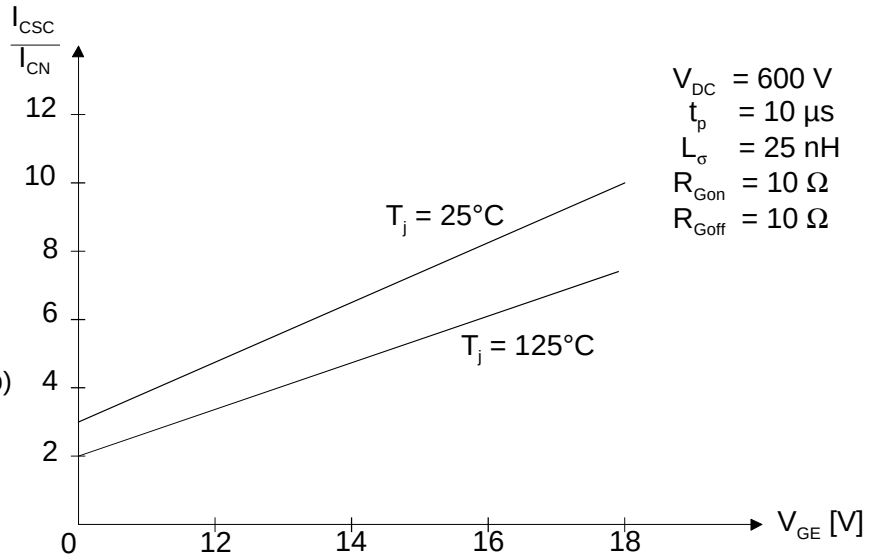


Figure 3.56 SOA at short circuit of an NPT-IGBT (SC SOA)
a) Normalized short-circuit current versus collector-emitter voltage (SKM100GB123D)
b) Normalized short-circuit current versus gate-emitter voltage (general)

The following important boundary conditions have to be fulfilled to guarantee safe operation:
- the short circuit has to be detected and turned off within max. 10 µs,
- the time between two short circuits has to be at least 1 second,
- the IGBT must not be subjected to more than 1000 short circuits during its total operation time.

Figure 3.56b shows the influence of gate-emitter voltage and junction temperature on the stationary short-circuit current.
Short circuit I and II will cause high power dissipations in the transistor, which will increase the junction temperature. Here, the positive temperature coefficient of the collector-emitter voltage has a favourable effect (this also goes for the drain-source voltage), since it causes reduction of the collector current during stationary short circuit (see Figure 3.56b).

Possibilities for reliable detection of fault currents and limitation of occurring overvoltages are summarized in chapter 3.6.3.

3.6.3 Fault detection and protection

Errors in inverters may be detected at various points, and the reaction to detected errors may be very differently.
We are talking about fast protection, if the error is detected within the switch itself and the switches are turned off directly by the driver. The total response time of the switch may possibly be only some 10 nanoseconds.
In case of error detection outside the switches firstly an error signal is transmitted to the control board, where a reaction to the error is triggered. This is called slow protection. The running processes are even related to converter control (e.g. the system's reaction to overload).
Modern converters mostly combine slow and fast protection procedures depending on the specific application.

A comprehensive comparison of protection concepts is included in [194].

3.6.3.1 Detection and reduction of fault currents

Detection of fault currents

Figure 3.57 shows a voltage source inverter circuit. Here, the measuring points are marked where fault currents can be detected.

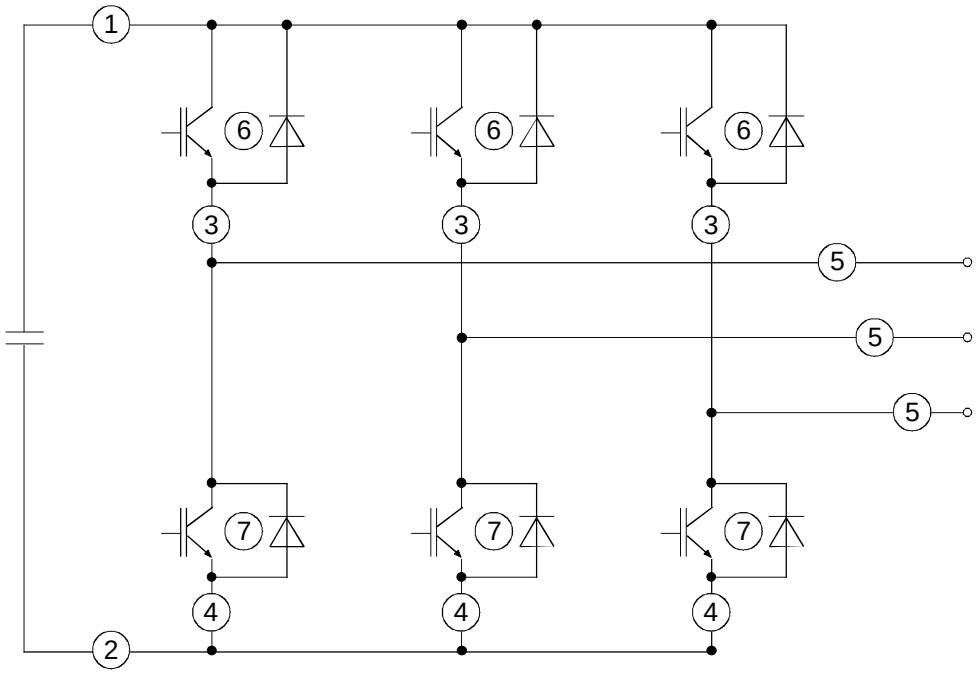


Figure 3.57 Voltage source inverter (VSI) with detection points for fault currents

Fault currents can be designed as follows:
Overcurrent: detectable at points 1-7
Arm short circuit: detectable at points 1-4 and 6-7
Load short circuit: detectable at points 1-7
Ground short circuit: detectable at detection 1, 3, 5, 6 or by calculation of the difference between 1 and 2

Principally, controlling short-circuit currents requires fast protection measures realizing direct control on the driver output stage, since the transistor switch has to turn off within 10µs after the short circuit has occurred. For this, fault currents may be detected at detection points 3, 4, 6 and 7 (with OCP-drivers also at detection point 5, see chapter 3.5.8).

Measurements at points 1-5 may be taken by means of measuring shunts (e.g. integrated in MiniSKiiPs) or inductive measuring current transformers (e.g. in OCP-SKiiPs and OCP-MiniSKiiPs).

Measuring shunt:

- simple measuring method,
- requires low-resistance (10...100 mΩ), low-inductance power shunts,
- measuring signal is highly sensitive to interferences,
- measuring values are not available with potential isolation.

Measuring current transformers:

- much more complicated realization compared to measuring shunt,
- Interference susceptibility of measuring signal is lower than with measuring shunt,
- measuring values are available with potential isolation.

At detection points 6 and 7 fault currents are detected directly at the IGBT/MOSFET-terminals. Here, protection methods are v_{CEsat} or $v_{DS(on)}$-monitoring (indirect measuring method) and current sensing, in case a sense-IGBT is used (direct measuring method). Figure 3.58 shows the principle circuits.

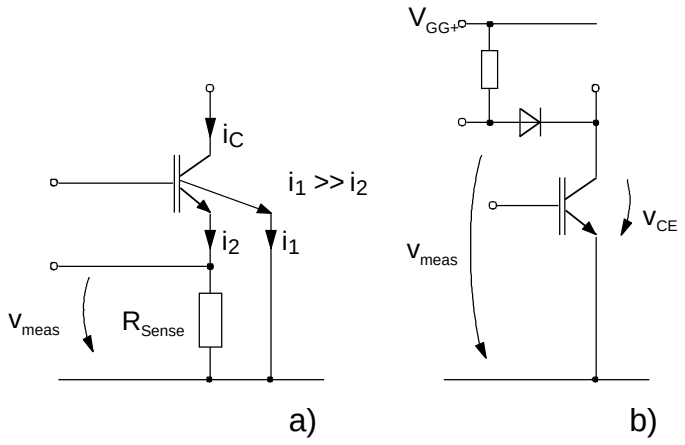


Figure 3.58 Fault current detection by a) current sensing and b) v_{CEsat}-monitoring

Current sensing with sense-IGBT:

In a sense-IGBT a few cells are combined to a sense-emitter generating two parallel current arms. Information is given by the conducted collector current as soon as it passes the measuring resistor. At $R_{Sense} = 0$ the current division ratio between both emitters is ideal, corresponding to the ratio of number of sense-cells to total number of cells. If R_{Sense} is increased, the current conducted in the measuring circuit will be reduced by feedback of the measuring signal.

Therefore, resistance R_{Sense} should be within a range of 1 - 5 Ω to obtain a sufficiently exact measuring result of the collector current.

If the turn-off current threshold value is only slightly more than the transistor rated current, the current monitoring has to made ineffective during turn-on of the IGBT because of the reverse-recovery current peak of the free-wheeling diode (in hard switching topologies).
For very high sense-resistances ($R_{Sense} \rightarrow \infty$) the measuring voltage corresponds to the collector-emitter saturation voltage, so that current sensing acts as a v_{CEsat}-monitoring.

V_{CEsat}-monitoring:

V_{CEsat}-monitoring makes use of the relationship between collector current and forward voltage indicated in the transistor datasheets (output characteristic).
The collector-emitter voltage is detected by a fast high-voltage diode and compared to a reference value. If the reference value is exceeded, the error memory will be set and the transistor will be turned off. The fast desaturation process in the transistor manages fast detection of short circuits. If the transistor is not desaturated by fault (e.g. if slowly increasing ground fault currents and overcurrents are involved), the application of v_{CEsat}-monitoring for fault detection will be restricted.
To guarantee safe turn-on of the IGBT during normal operation, v_{CEsat}-monitoring has to be gated until the collector-emitter voltage has fallen below the reference voltage (see chapter 3.5.4). Since no short-circuit protection is given during this period, the gating time must not exceed 10µs.
Temperature dependency of the output characteristic as well as parameter spreading have negative effects on v_{CEsat}-monitoring. However, the substantial advantage compared to current sensing with sense-IGBT is that this protection concept is applicable to every standard-IGBT/MOSFET.

Fault current reduction

Improved protection of the transistor switch can be achieved by reduction or limitation of high fault currents, especially with regard to short circuits and low-impedance ground fault circuits.

As explained in chapter 3.6.2, a short circuit of type II will generate a dynamic short circuit overcurrent due to the increase of the gate-emitter voltage because of high dv_{CE}/dt.
The amplitude of the short-circuit current may be reduced by clamping the gate-emitter voltage. Suitable circuit variants are given in chapter 3.6.3.2.
Apart from limitation of dynamic short-circuit overcurrents, stationary short-circuit currents may also be decreased by reducing the gate-emitter voltage (see Figure 3.56b of chapter 3.6.2). This will reduce transistor power losses during the short-circuit time. At the same time, overvoltage is decreased by turning off the lower short-circuit current. The principle is shown in Figure 3.59.

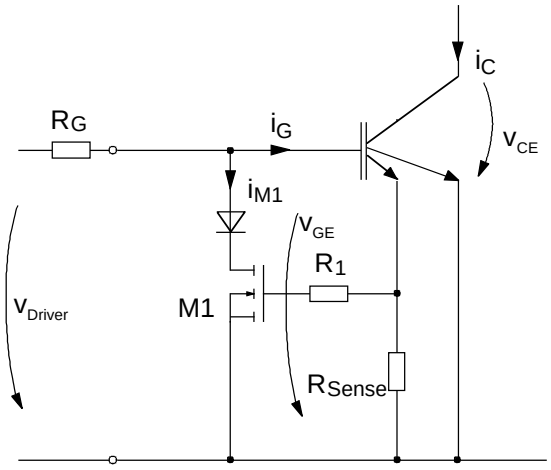


Figure 3.59 Short-circuit current limitation by reduction of gate-emitter voltage

This protection technique limits the stationary short-circuit current to about three times the rated current in rugged modules described under [281].

3.6.3.2 Overvoltage limitation

Overvoltage limitation between main terminals

Measures to limit overvoltages between main terminals (collector-emitter voltage, DC-link voltage) can be divided into passive snubber-networks, active clamping and dynamic gate control.

Independent of the kind of overvoltage limitation, the avalanche operation mode of MOSFETs can be utilized (see Figure 3.2). Please follow closely the limit ratings indicated in the datasheets or ask the manufacturer for corresponding limit ratings.

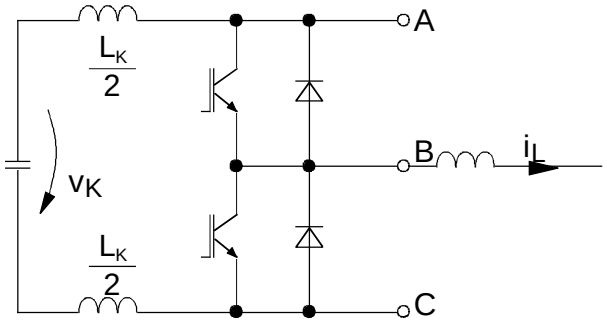
Passive snubber-networks

Passive networks (snubbers) are combinations of passive elements such as R, L, C, suppressor diodes, diodes, varistors etc.

In addition to chapter 3.8.2 the following explanations will consider variants, which are not responsible for switching loss reduction.

Figure 3.60 shows a summary of simple circuits.

Basic Circuit



Snubber Variants

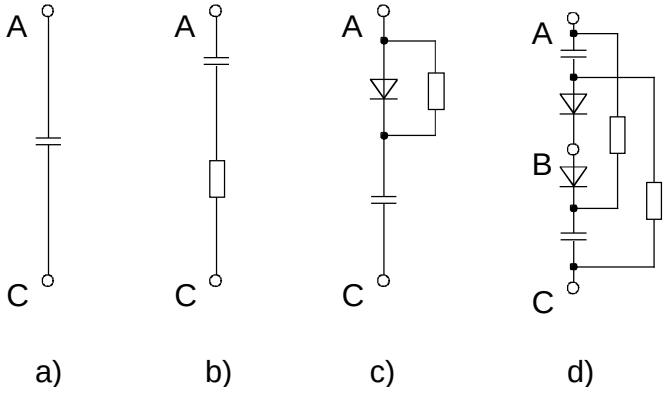


Figure 3.60 Passive overvoltage limitation networks

The principle of passive snubber-networks is to avoid induction of dangerous overvoltages due to the inductances of the commutation circuit L_K by attaching a capacitor which absorbs the energy stored in L_K ($E = L_K/2 * i^2$). The capacitor will be charged with the voltage difference $\Delta V^2 \approx L_K * \Delta i^2/C$ and will set a limit to overvoltages. The absorbed energy has to be discharged again between two charging processes to keep up the function of the network. With simple snubbers, this task is fulfilled by heat conversion in the snubber-resistors or by feedback to the DC-link capacitor.

The simplest method is to clamp the DC link voltage directly to the power module terminals by means of a capacitor (film capacitor or something similar). This measure is sufficient for many VSI applications. In this case, the capacitance values are up to 0.1 - 2 µF (Figure 3.60a).
To absorb parasitic oscillations between C and L_K, voltage clamping may be achieved by an RC-element (Figure 3.60b). This measure is recommended for low-voltage/ high-current applications (e.g. MOSFET-converters), to avoid parasitic change of the DC-link voltage polarity at the module terminals.
Figures 3.60c and d show some RCD-networks. The integrated fast diodes should feature low forward turn-on overvoltage and soft-reverse-recovery behaviour.
The snubber-network itself has to be laid out with minimum inductance.
Passive networks do not require any active components, which is an additional advantage to their simple topologies.
On the contrary, the overvoltage limit value can vary dependent on the operating point. Therefore, dimensioning has to be based on the worst case.

Active Clamping [161], [261], [302]

Active clamping of MOS-controlled transistors designates direct feedback of the collector-/drain-potential to the gate via a Zener-element. Figure 3.61 shows the basic principle and variants produced with the example of an IGBT-switch.

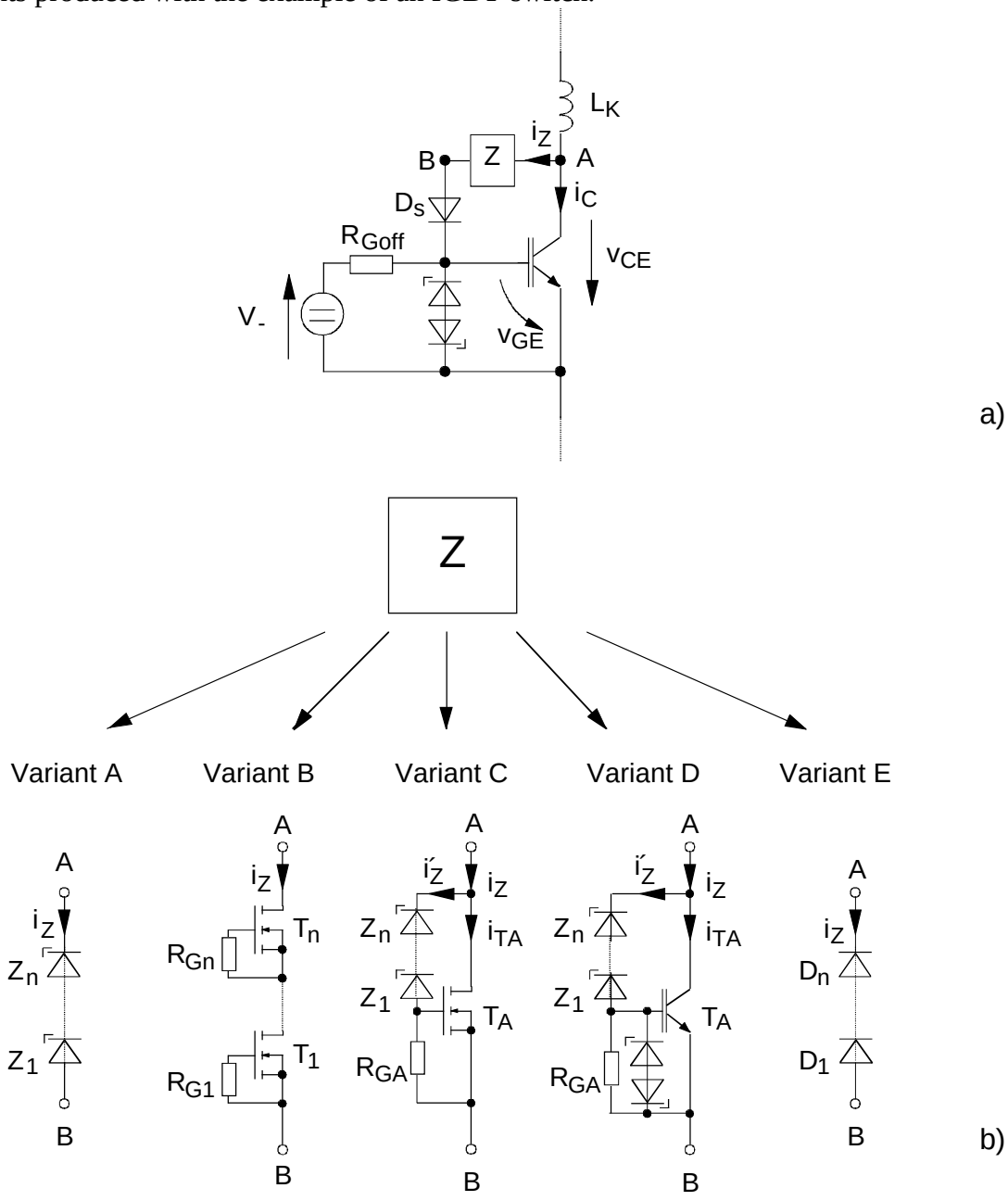


Figure 3.61 Basic principle (a) of active clamping and variants (b)

The feedback arm consists of a Zener-element Z and an attached diode D_s, which will stop current flow from driver to collector, when the IGBT is turned on.

If the collector-emitter voltage passes the avalanche breakdown voltage of the Zener-element, a current will be conducted to the IGBT gate via feedback coupling, which will raise the gate potential to a value given by the IGBT transfer and output characteristic ($i_c = f(v_{CE},v_{GE})$) (Figure 3.62). The clamping process will be continued as long as current is impressed by the series inductance. The voltage applied to the transistor being determined by the current-voltage characteristic of the Zener-element. The transistor operate in the active area of its output

characteristic (!!safe operating area!!) and converts the energy stored in L_K to heat (Figure 3.62). Figure 3.62 explains these correlations by depiction of typical characteristics.

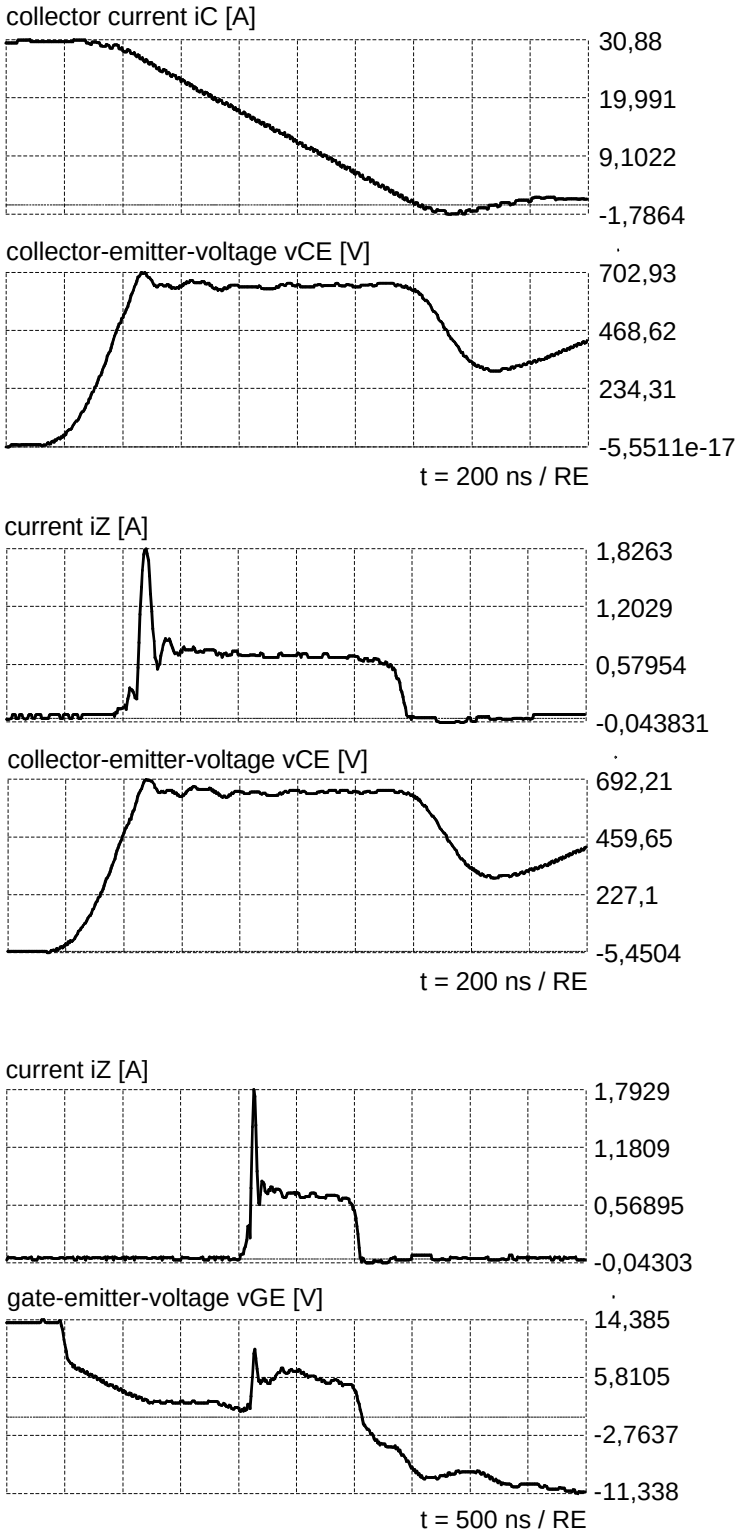


Figure 3.62 Typical current and voltage characteristics during active clamping (variant A),(v_K = 400 V, v_{cl} = 640 V, i_{C0} = 30 A, L_K = 10 µH, T_j = 30°C, V_- = -15 V, SKM100GB123D)

The gate charge peak current necessary for increasing the gate voltage at the beginning of the clamping process is clearly shown in Figure 3.62.

Selection of the suitable variant produced is dependent on the average power dissipation in the Zener-element. This is based on the following principle: the higher the voltage difference between commutation voltage and clamping voltage, the lower the power dissipations in the clamping circuit.
Another criterion of selection might be the rate of rise of the Zener-characteristic (Figure 3.63).

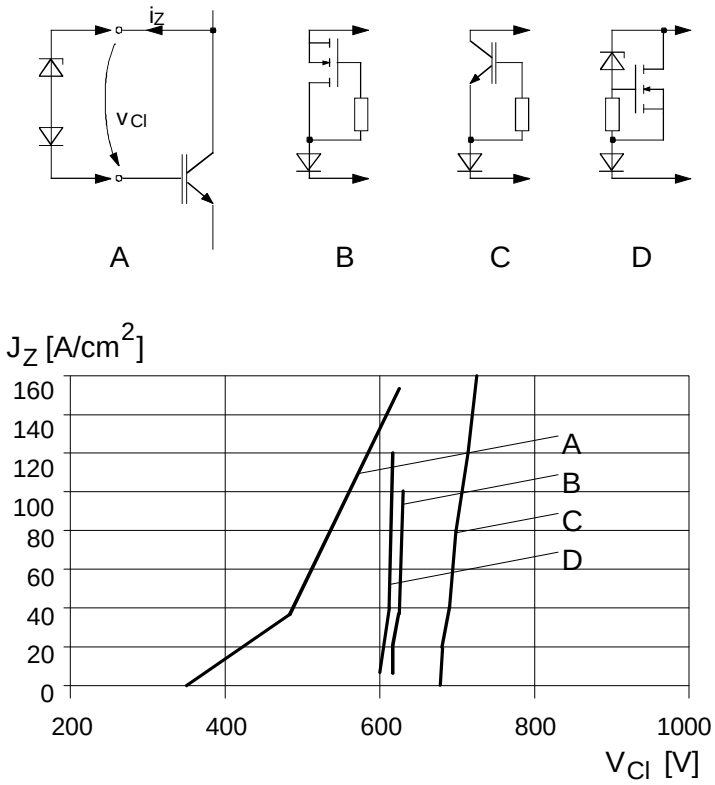


Figure 3.63 Static characteristics of selected Zener-elements [194]
A: Suppressor diode 06KE350, B: BUZ90 during avalanche breakdown
C: BUP400 during avalanche breakdown, D: BUZ78 as amplifier

Variant A of Figure 3.61 can be realized very easily and may be used at low clamping energy applications (e.g. in pulsed voltage source converters).
The MOSFETs and diodes in variants B and E are operated in avalanche-mode.
In variants C and D the MOSFET/ IGBT serves as amplifier for the Zener current, variant D being characterized by an especially high ruggedness.

Features of active clamping are summarized as follows:
- simple circuit arrangement,
- the transistor to be protected is part of the protection itself and converts the main share of energy stored in L_K in the clamping process,
- there is no need for power resistors and snubber capacitors,
- steep clamping characteristic,
- the switch voltage to be limited is independent of the operating point of the inverter,
- the principle does not require a separate power supply,
- conventional drivers may be applied,
- overvoltages during reverse-recovery-di/dt of the inverse diodes are limited at the same way,
- possibility to equip either every single transistor switch with a clamping circuit or to attach one central clamper for one or several pairs of switches.

The principle of active clamping has not been utilized industrially so far, but for short-circuit protection of inverters with DC-voltage links, where clamping is done only in case of faults of the inverter at relatively low energies.
Investigations described under [161] show, however, that the active clamping process would also turn out to be advantageous under periodic operation conditions of ZCS-switch mode power supplies, where high energies are involved (clamping frequency: 15...30 kHz). All in all, the possibilities and limits of this protection concept will still have to undergo extensive research and development. This goes especially for periodic short-term operation of IGBTs and MOSFETs in the acitve region of the output characteristic.

Dynamic gate control

In the procedure of dynamic gate control the di/dt and dv/dt and the consequently induced overvoltages are directly determined by the driver.
Another more simple protection procedure of dynamic gate control is slow turn-off of IGBTs and MOSFETs in case of overcurrents or short circuit applying higher gate series resistors (e.g. driver stage SEMIKRON SKHI 23) or turn-off by defined current (current source control) (Figure 3.64).

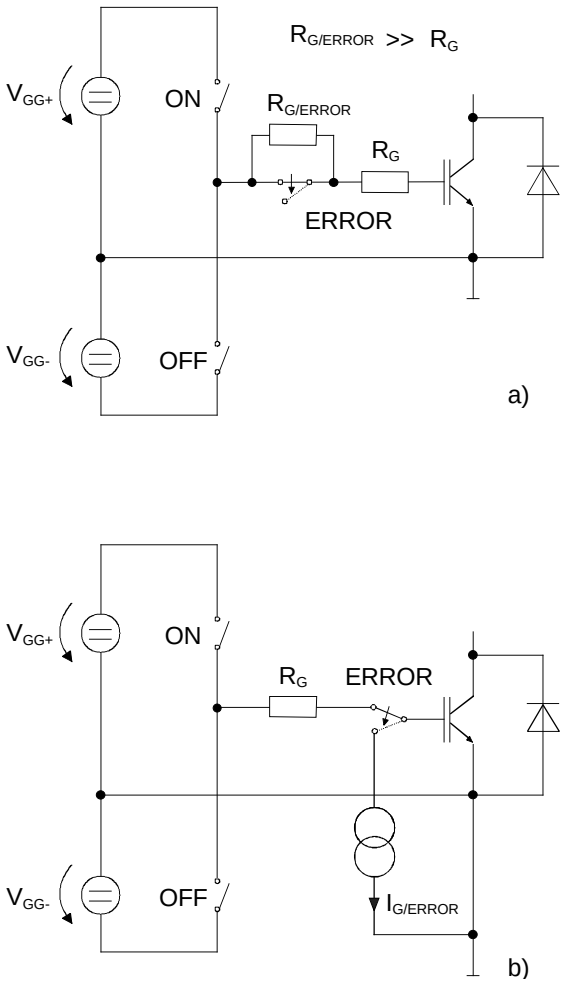


Figure 3.64 Possible slow turn-off procedures in case of converter fault operation
a) Increased R_{Goff}
b) Current source control

In the drivers introduced under [9], [47] and [61] the IGBT/MOSFET dv/dt and di/dt are detected and fed back to the driver (Figure 3.65).

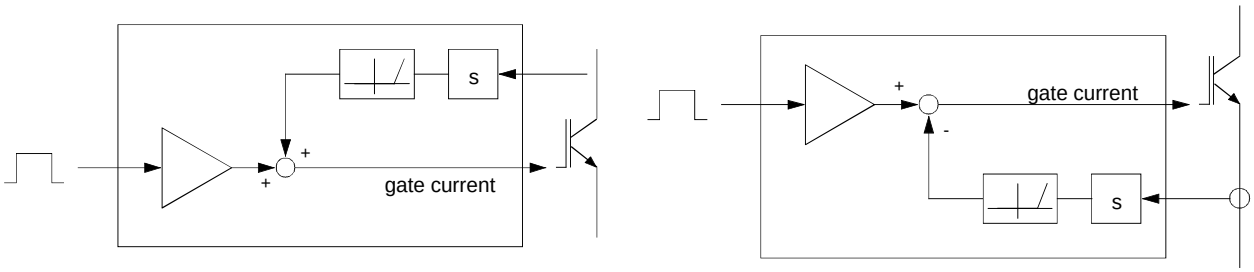


Figure 3.65 Direct dv/dt- and di/dt-detection

Here, the information on di/dt or dv/dt is got by inductance at the emitter or by capacitance at the collector, respectively.

Overvoltage limitation between control terminals

Overvoltage limitation between control terminals is required for keeping up the maximum gate-emitter/ gate-source voltage on the one hand, and for limitation of the dynamic short-circuit current amplitude on the other hand.
Figure 3.66 shows a summary of simple circuit variants. For the sake of optimized efficiency the limitation circuits should be laied out for low inductance and be attached as close as possible to the gate.

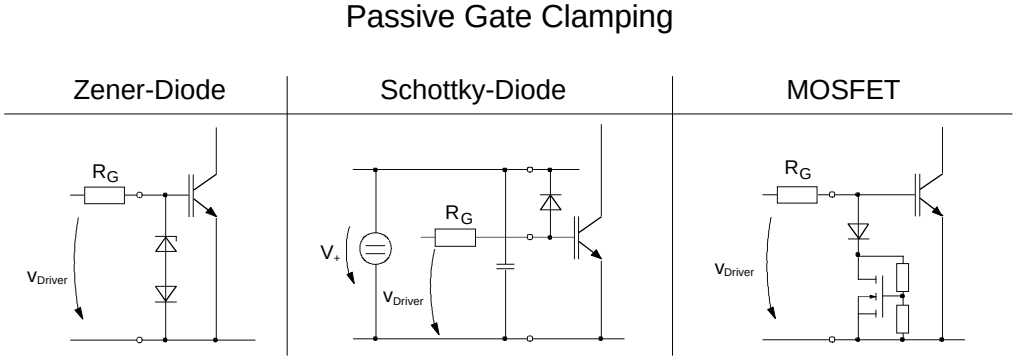


Figure 3.66 Simple gate voltage limitation circuits [194]

3.6.3.3 Overtemperature detection

Direct measurement of the junction temperature is only possible, if the temperature sensor is attached very close to the semiconductor component (e.g. by monolithic integration or by connecting of the temperature sensor and the power semiconductor chip).
Information on temperature can then be got from the evaluation of diode or thyristor blocking currents.
However, technologies of that kind have only been applied in smart-power components so far.

In transistor power module applications temperatures are measured either outside the module from the heatsink or inside the module by temperature-dependent resistors close to the power semiconductor chips (e.g. with SEMIKRON SKiiP/ MiniSKiiP).
Because of the given thermal time constants, only information about the average temperature is given (dynamic temperature measurement is not possible).

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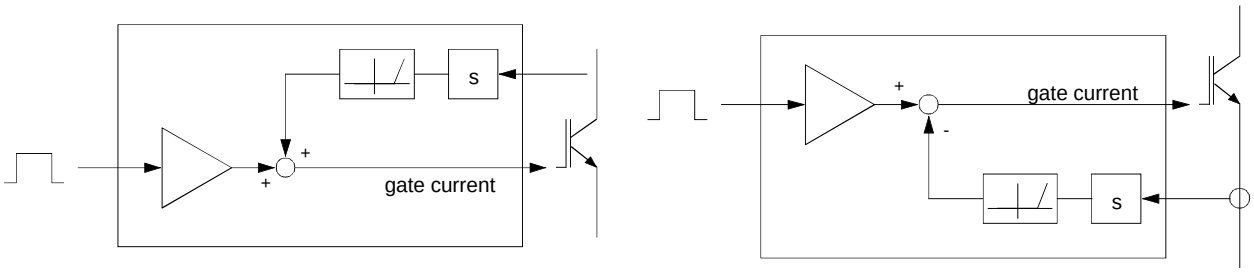

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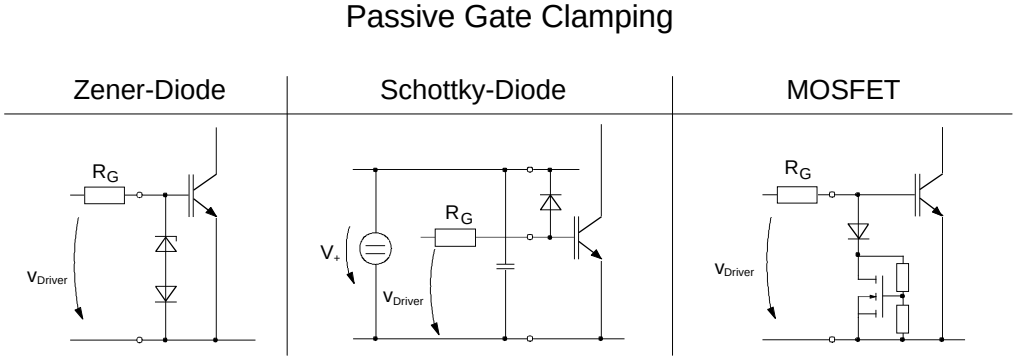

Figure 3.66 Simple gate voltage limitation circuits [194]

3.6.3.3 Overtemperature detection

Direct measurement of the junction temperature is only possible, if the temperature sensor is attached very close to the semiconductor component (e.g. by monolithic integration or by connecting of the temperature sensor and the power semiconductor chip).
Information on temperature can then be got from the evaluation of diode or thyristor blocking currents.
However, technologies of that kind have only been applied in smart-power components so far.

In transistor power module applications temperatures are measured either outside the module from the heatsink or inside the module by temperature-dependent resistors close to the power semiconductor chips (e.g. with SEMIKRON SKiiP/ MiniSKiiP).
Because of the given thermal time constants, only information about the average temperature is given (dynamic temperature measurement is not possible).

If given reference values (which are extremely application-specific) in converters are exceeded, the system can react by immediate turn-off or by operation with reduced power.

3.7 Parallel and series connection of MOSFET, IGBT and SKiiPPACK modules

3.7.1 Parallel connection

3.7.1.1 Problems of current sharing

To improve the current capability of power electronic switches, IGBT and MOSFET modules can be connected in parallel.
By paralleling power modules, the transistors and necessary inverse diodes or free-wheeling diodes are also paralleled. As parallel connection of fast diodes had already been dealt with in chapter 1.3.5.2, only special characteristics of IGBTs/ MOSFETs will be discussed to in the following.

Maximum utilization of the switch generated by parallel connection will only be achieved in the case of ideal static (i.e. in the forward operation) and dynamic (i.e. at the moment of switching) symmetrization of the single modules (current sharing).
Therefore, optimal symmetry conditions are of major importance for parallel connections in practice.

Current sharing is mainly effected by the following factors:

Factor	Influence on	
	static symmetry	dynamic symmetry
<u>IGBT/MOSFET-parameters</u>		
$v_{CEsat} = f(i_C, v_{GE}, T_j)$ or $R_{DSon} = f(v_{GS}, T_j)$	**x**	
$i_C = f(v_{GE}, T_j)$ or $i_D = f(v_{GS}, T_j)$		**x**
$v_{GE(th)}$ or $v_{GS(th)}$		**x**
$t_{d(on)}$, $t_{d(off)}$, t_r, t_f (in connection with driver parameters)		**x**
<u>Commutation circuit</u>		
Total loop inductance (inside the module + outside the module)	**(x)**	**x**
<u>Driver circuit</u>		
Output impedance of driver (including gate series resistances)		**x**

Total loop inductance (inside the module + outside the module)	**x**
Driver circuit inductance carrying collector/ drain current	**x**

Influence of saturation voltage and $R_{DS(on)}$ respectively

The on-state voltage induced during stationary forward on-state is the same for both paralleled transistors. Current distribution is dependent on the tolerances of the output characteristics.
Figure 3.67 shows how the total load current is distributed over two paralleled IGBTs with different output characteristics.

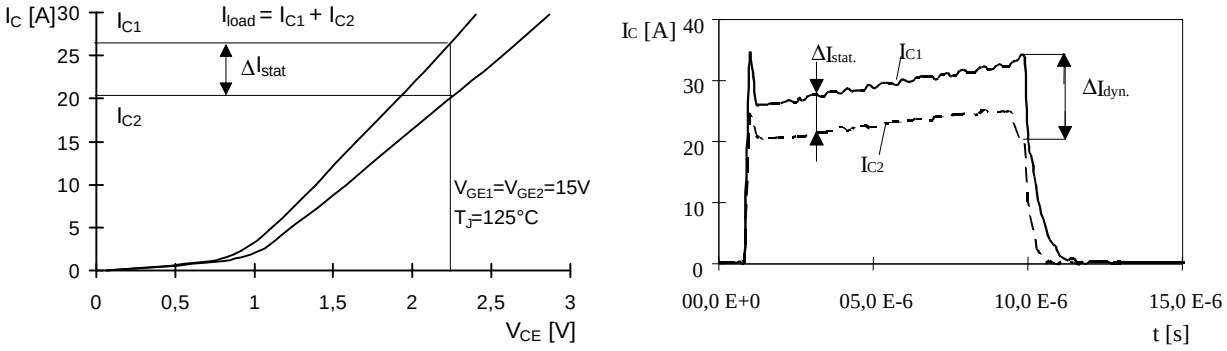

Figure 3.67 Static current distribution over two paralleled IGBTs with different output characteristics

In the beginning, the major current share is conducted by the transistor with the lower saturation characteristic, which is therefore subject to higher forward and switching losses, and, by consequence, the junction temperature will increase rapidly.
In this respect, the temperature coefficient (TC) of the saturation voltage is of decisive importance. If the TC is positive, i.e. if the saturation voltage rises together with the temperature, the current will be shifted to the transistor which had carried the minor current share in the beginning. Finally, the current will (ideally) be evenly distributed over the paralleled transistors.
Therefore, power semiconductors with a positive TC are preferably used for parallel connections.
The TC of NPT IGBTs is positive over almost the whole rated current range. The same goes for the R_{DSon} of MOSFETs, featuring a positive TC by principle.
In contrast to that, the TC of PT IGBTs is negative over almost the whole rated current range. Here, good thermal coupling between paralleled modules is substantial.

Influence of the transfer characteristic $i_C = f(v_{GE}, T_j)$ and $i_D = f(v_{GS}, T_j)$ respectively

Deviations in the transfer characteristics, threshold voltages and switching delay times will lead to dynamic asymmetries at the moment of switching and, consequently, to different switching losses, especially during turn-off.

Figure 3.68 shows the example of deviating transfer characteristics of paralleled NPT IGBTs and thereby caused dynamic current asymmetry during turn-off.

Due to the common gate voltage during the Miller process, the IGBT with the steeper transfer characteristic will conduct the major current share during dynamic current distribution and is therefore subject to higher turn-off power dissipation.

While the positive on-state voltage TC of NPT-IGBTs is supporting parallel connections, the steep transfer characteristic and high switching speed will have negative effects on dynamic symmetry.

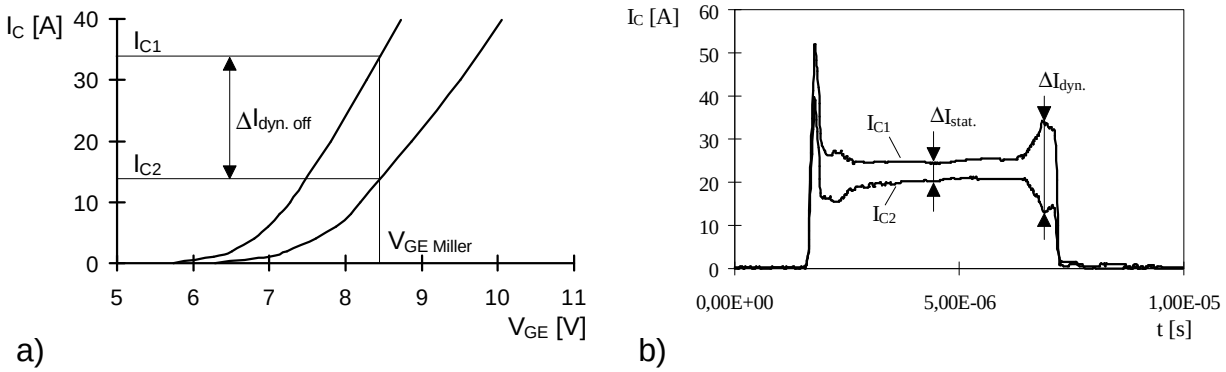

Figure 3.68 a) Transfer characteristics of two paralleled NPT-IGBTs
b) Dynamic current distribution during switching

Furthermore, Figure 3.68 makes it clear that, in addition to the transfer characteristics, the deviations of turn-on losses of IGBTs/ MOSFETs are basically determined by the turn-off behaviour of the free-wheeling diodes.

Influence of loop inductance in the commutation circuit

Following the explanations in chapter 3.4.1, turn-on and turn-off power dissipations of power semiconductors are determined by the commutation circuit inductance L_K (loss reduction effect during turn-on, generation of switching overvoltage during turn-off).
Paralleling of switches is always equivalent to paralleling of commutation circuits. If commutation circuits are subject to different loop inductances, the switching speed of fast power semiconductors may be differently, which would cause dynamic asymmetries. Therefore, a strictly symmetrical layout of the commutation circuit should be realized.

Influence of the driver output impedance (including gate series resistances)

Impedance deviations of the driver circuits of paralleled transistors have to be minimized. Existing deviations will lead to non-simultaneous switching and will contribute to unbalanced distribution of switching losses.

Influence of loop inductance of the driver circuit

In combination with transistor input capacitances, the driver circuit loop inductance can generate heavy oscillations, which might even spread between paralleled transistors (see chapters 3.7.1.2 and 3.4.1).
To avoid such parasitic oscillations, principally any loop inductance in the driver circuit has to be minimized.

Influence of the collector-/drain-current-carrying inductance of the driver circuit

Fast alterations of the collector-/ drain-current during switching will induce voltages to the driver circuit inductance, where the main current is conducted; these voltages are counteractive to the gate charge or gate discharge, respectively (emitter-/ source negative feedback). The consequent deceleration of the switching process will increase switching losses.
With respect to paralleling of transistors, different values of these inductances might contribute to asymmetrical distribution of switching losses.

3.7.1.2 Module selection, driver circuit, layout

The following recommendations with reference to module selection, driver and layout for paralleling of IGBTs and MOSFETs can be concluded from chapter 3.7.1.1.

Module selection

As for proper handling of dynamic symmetrization, NPT IGBTs are especially suitable for parallel connection because of the positive TC of their saturation voltage. Furthermore, they are outstanding for low tolerances and they are less temperature-dependent in their parameters.

Driver circuit

Figure 3.69 shows a proposal for the driver circuit layout for paralleling of IGBTs. The circuit is driven by one common driver unit.
In addition to the common gate series resistances R_{Gon} and R_{Goff} integrated in the driver, the resistances R_{Gonx} and R_{Goffx} damp parasitic oscillations between the gate-emitter/ gate-source circuits. Moreover, they reduce the negative effects of the different transfer characteristics.
R_{Gonx} and R_{Goffx} should be dimensioned with about 0.5 ...2 Ω.

The resistances R_{Ex} will suppress balancing currents via auxiliary emitters. They should be dimensioned with about 0.5 Ω.

The resistances R_{Cx} serve to determine the average actual v_{CE}-/v_{DS}-value in case overcurrent- and short circuit protection is based on v_{CEsat}-/v_{DS} -evaluation.
They should be dimensioned with about 47 Ω.

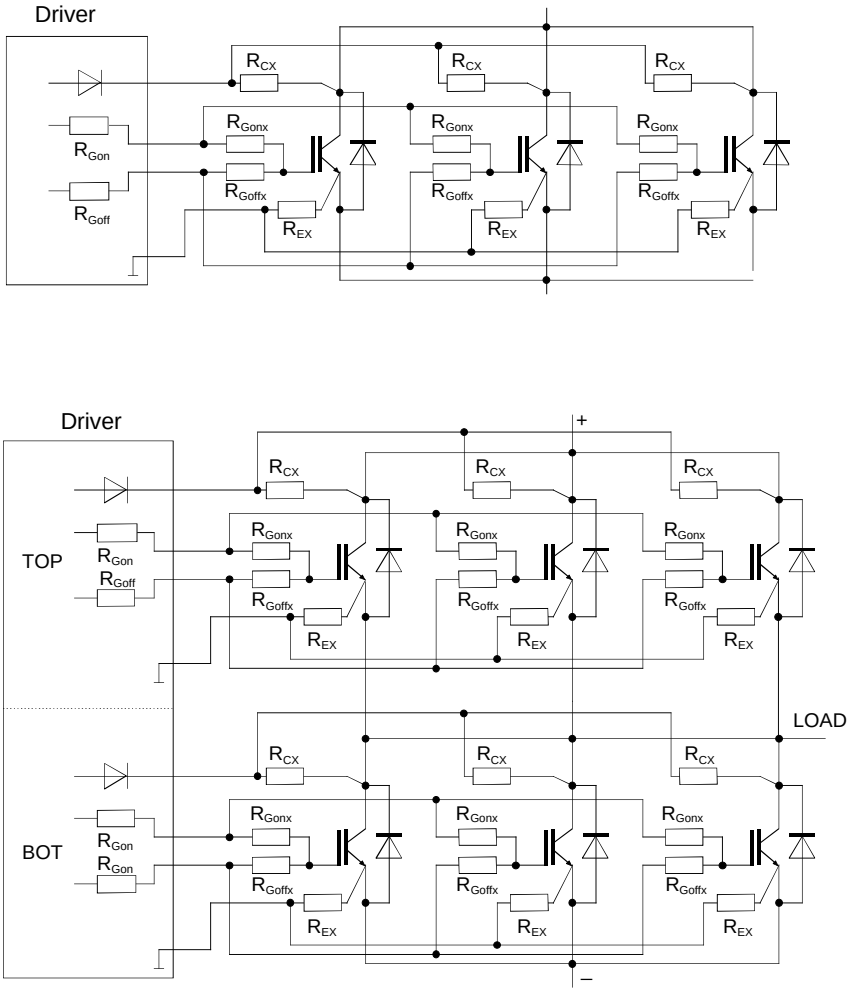

Figure 3.69 Parallel connection of single and dual IGBT modules

If paralleled transistors are to be driven by separate driver units, the driver units should feature identical signal propagation times and output parameters.

Layout

All power and driver circuits within the parallel circuit have to be laied out with minimum loop inductance and strictly symmetrical wiring.

Modules have to be mounted to a common heatsink close to each other to guarantee optimal thermal coupling (also because of symmetrization of inverse and free-wheeling diode).

Modern power modules are characterized by minimized internal inductances in the power and driver circuit of only some nH. However, since different module constructions will also show different inductance ratings, only modules of the same construction type should be connected in parallel.

Derating

Even if all conditions for optimal module selection, driver circuit and layout design have been fulfilled, an ideal static and dynamic symmetrization will not be achievable.
Therefore, derating has to be considered with respect to the total rated load current of the switches. From practical experiences in different applications a derating of about 15-20 % can be advised.

Example: Paralleling of three IGBT-modules with v_{CE} = 1200 V/i_C = 300 A
Rated current of the parallel circuit: i_{Ctot} = (3∗300 A) ∗ (0.8 ..0.85) = 720..765 A.

3.7.1.3 Parallel connection of SKiiPPACK modules

SKiiPPACK modules integrate power semiconductors and complete driver circuits in one housing. In the case of direct paralleling of modules, symmetrization will be determined only by the power layout (inductances, cooling system).
Differences in signal propagation times and driver output impedances of the single modules might cause substantial asymmetries.

The “Parallel-Board“ SKHBP2 and SKHBP4 assemblies by SEMIKRON support paralleling of 2 and 4 SKiiPPACK-modules, respectively.

Figure 3.70 shows a block diagram with a connected SKHBP2 for paralleling of two SKiiPPACK-modules.

The SKHBP2 is responsible for the following main functions:
- Generation and synchronization of control signals for single modules out of one controller signal,
- Generation of a common arm interlock time,
- Short-pulse suppression,
- Common ERROR-memory with RESET-function,
- Collection of feedback signals of the single modules and transfer to the controller (error detection, analogous temperature output, for OCP-SKiiP: generation of the total actual load current value).

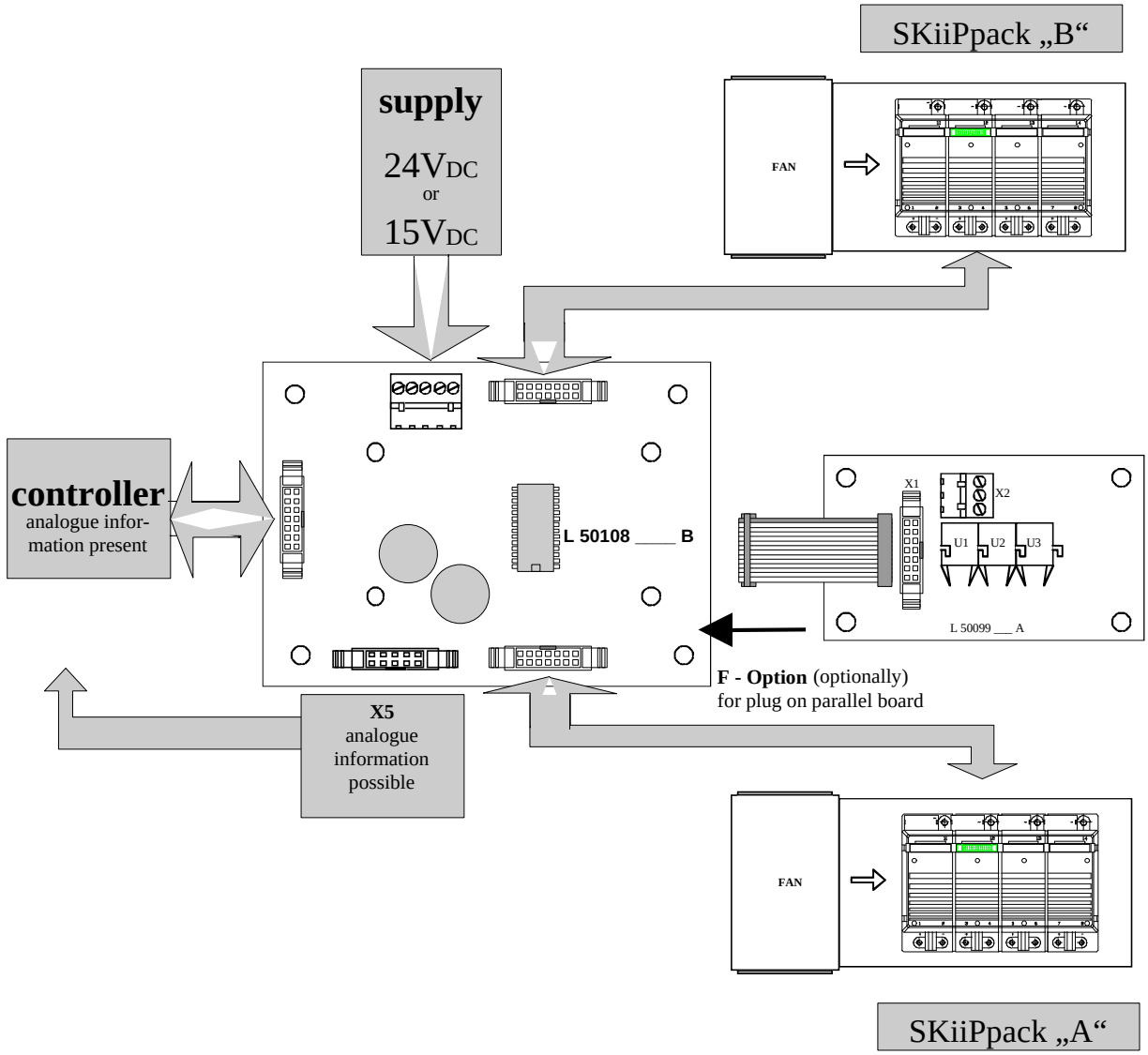

Figure 3.70 Parallel connection of two SKiiPPACK-modules with “Parallel-Board SKHBP2”

Despite connection of the parallel board, small differences in switching times might occur due to differing signal propagation times within the single modules.
The consequent dynamic asymmetries may be minimized by series inductances (dynamic decoupling) in the connected load paths.
These inductances might figure up to some Micro-Henry, and in many applications the inductances of the load connection cables between output of the single modules and their point of common connection can be utilized (see Figure 3.71).

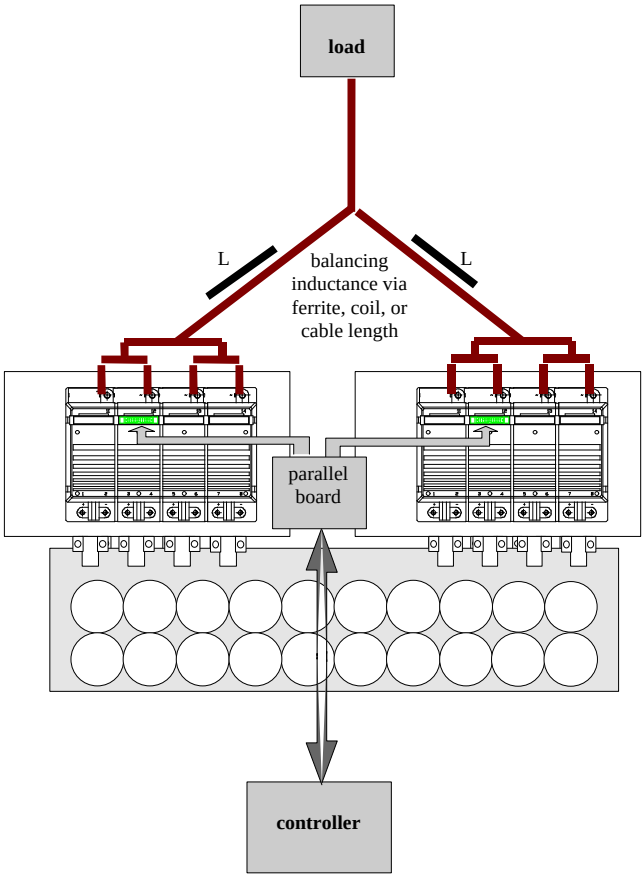

Figure 3.71 Dynamic decoupling of paralleled single modules by the inductances of the load connection cables

As for total derating please follow the explanations in chapter 3.7.1.2.

3.7.2 Series connection

3.7.2.1 Problems of voltage sharing

To increase the blocking voltage of power electronic switches, IGBT and MOSFET modules may be connected in series.
By series connection of power modules, the transistors and necessary inverse diodes or free-wheeling diodes are connected in series. As series connection of fast diodes has already been dealt with in chapter 1.3.5.1, only special problems of IGBTs/ MOSFETs will be referred to in the following.

Maximum voltage utilization of the switch generated by series connection will only be achieved in case of ideal static (i.e.during blocking state) and dynamic (i.e. in the moment of switching) symmetrization of the single modules.
Therefore, optimal symmetry conditions are of major importance for the application of series connections in practice.

Symmetrization is mainly influenced by the following factors:

Factor	Determination of	
	static symmetry	dynamic symmetry
IGBT/MOSFET-parameters $i_{CES} = f(v_{CE}, v_{GE}, T_j)$ or $_{DSS} = f(v_{DS}, v_{GS}, T_j)$	**x**	
$v_{GE(th)}$ or $v_{GS(th)}$		**x**
$t_{d(on)}$, $t_{d(off)}$, t_r, t_f (in connection with driver parameters)		**x**
Driver circuit		
Output impedance of driver (including gate series resistances)		**x**
Total loop inductance (inside the module + outside the module)		**x**
Driver circuit inductance carrying collector/ drain current		**x**
Driver signal propagation times		**x**

Reasons for static asymmetry

During stationary off-state of IGBTs / MOSFETs the conditions of symmetry are determined by the blocking characteristics of the transistors connected in series.
The higher the blocking current of a transistor, or, in turn, the lower the blocking resistance, the lower is the voltage taken up by the transistor, if it is connected in series.
The blocking current temperature coefficient for IGBTs and MOSFETs is positive, i.e. the blocking current will increase linear to the rising temperature.

Reasons for dynamic asymmetry

All factors determining dynamic symmetrization mentioned above will finally lead to deviating switching times of the transistors connected in series. The transistor turning off first and the one turning on last will be burdened with the highest voltage and, consequently, with the highest switching losses. Exceeding the maximum admissible transistor voltage must be avoided by the countermeasures discussed in the following chapter.

3.7.2.2 Module selection, driver circuit, snubber networks, layout

Module selection and layout

Optimal symmetry conditions are always based on minor spreadings of parameters of the modules connected in series.
Please avoid series connection of different types of modules or modules produced by different manufacturers.

The power and driver circuits have to be laid out principally in consideration of minimum parasitic inductances and strictly symmetrical arrangements (also see chapter 3.7.1).

Static symmetrization

To achieve optimal static symmetrization conditions, the influence of differing blocking currents has to be decreased by paralleling of resistors.
Following chapter 1.3.5.1, the current conducted through the parallel resistor may be rated to about 3-5 times as high as the transistor blocking current.

Example: Series connection of two IGBT-modules SKM400GA173D
v_{CES} = 1700 V, i_{CES} (v_{CES}, T_j = 125°C) = 4.5 mA

Application of a DC-link voltage of 2400 V will result in:
R_p = 75..125 kΩ P_{Rp} = 19..11 W

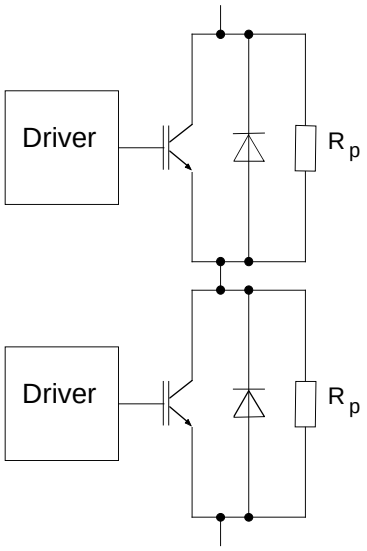

Figure 3.72 Static symmetrization with parallel resistors

Dynamic symmetrization

Optimal dynamic symmetrization is always based on minimum deviations of signal propagation times of the driver stages.

Passive snubber-networks

RC or RCD networks can support dynamic symmetrization very efficiently (see Figure 3.73). These networks reduce, and thus balance dv/dt speed during switching (compensation of non-linear component junction capacitances). However, the high reliability achieved by attachment of RC or RCD networks faces the requirement for more passive power components, which have to be laid out for high voltages. Snubber networks are responsible for conversion of partly substantial extra losses. Another disadvantage is that the quantitative performance is dependent on the actual operating point of the circuit.
In contrast to that, there is no need for additional control circuitry and the use of standard driver stages will be sufficient.
If passive networks are combined with active symmetrization technologies, they may be laid out with lower parameters. A combination of active symmetrization and passive network is introduced under [45] and [236]. Here, the RC networks are laid out with R = 3.3 Ω and

C = 15 nF at a DC link voltage of 2.4 kV for series connection of four 1200 V/ 600 A IGBT-switches.

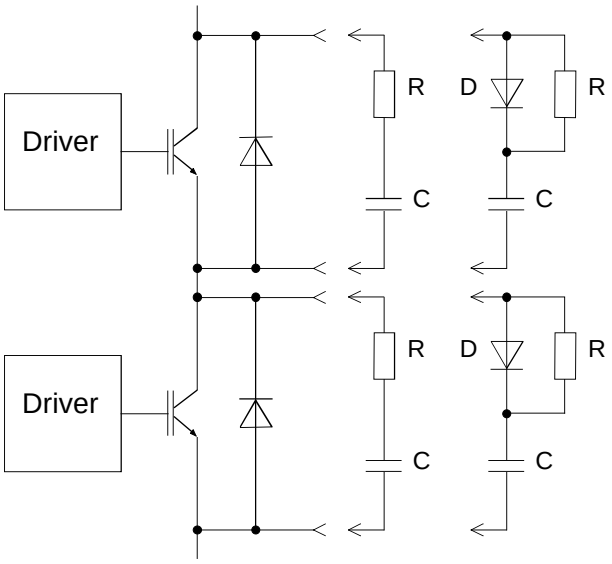

Figure 3.73 Passive networks

Active symmetrization measures

Switching time correction [61]

Figure 3.74 shows one possibility of producing dynamic voltage symmetrization according to the principle of switching time correction via delay times. This method does not require any additional passive power components. There are no extra losses generated in the IGBTs/ MOSFETs.

On the other hand, this method demands high standards with respect to driver and control circuit.

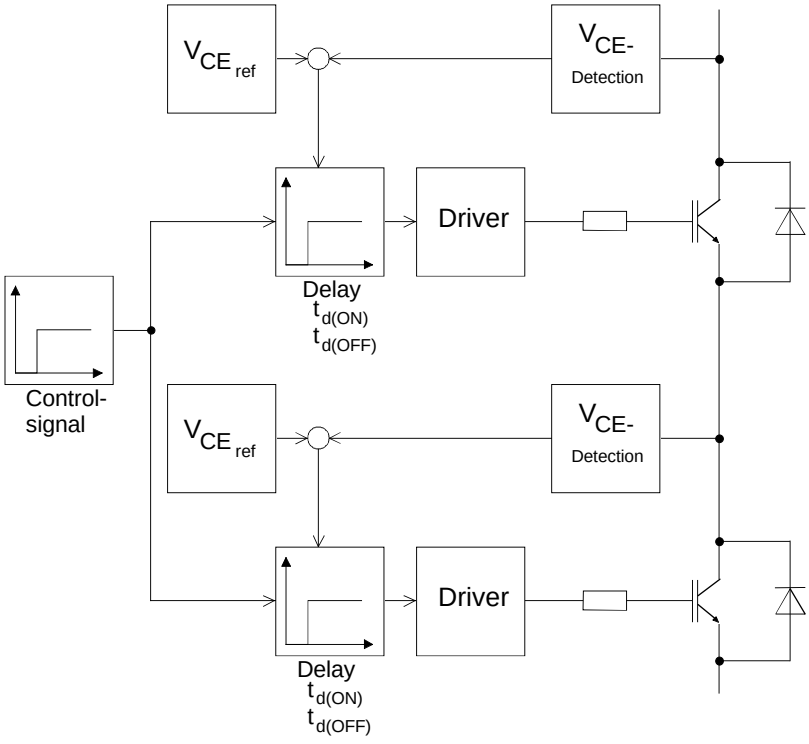

Figure 3.74 Principle of switching time correction

dv/dt – control [61], [9]
The principle of dv/dt-control is that a reference value for the dv/dt speed of single modules during switching is compared to the actual values by the driver; the difference between those values is transmitted to the driver output stage.
In this respect, the exact and reproduceable capacitive coupling or feedback of the actual dv/dt-values might be problematic.
If the dv/dt-reference value is lower than the „natural“ dv/dt during hard switching, additional losses will be generated in the power transistors.
Consequently, the driver layout has to be more sophisticated, standard drivers may no longer be used.
Similarly, di/dt control with inductive feedback of the di/dt speed of IGBTs / MOSFETs may be achieved [9], [61].

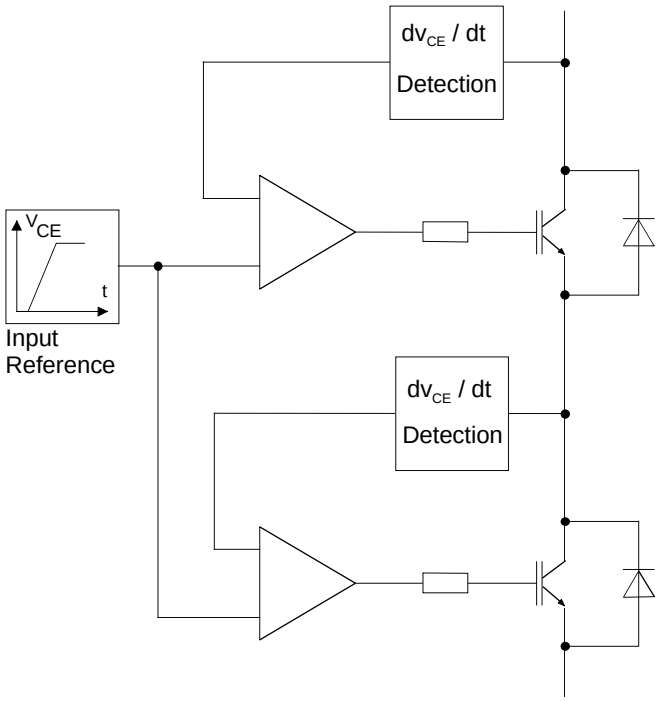

Figure 3.75 Dynamic voltage symmetrization by dv/dt-control

Active voltage limitation / active clamping [37], [161], [236], [261]
The process of active clamping is characterized by indication of the collector-emitter voltage or the drain-source voltage, respectively, and feedback to the gate by a Zener-element (see chapter 3.6.3.2, Figure 3.76).
If the transistor voltage passes the given maximum voltage, the gate voltage will be increased to such an extent, that the operating point is shifted to the active region of the output characteristic in accordance with the collector-/ drain-current conducted.
The additional losses generated in the transistor during active clamping are relatively low.
Active clamping has no influence on symmetrization of the switching edges.
This method works without time delays, the limitation voltage value being independent of the operating point of the inverter.
Moreover, it is of advantage that almost any standard driver may be equipped with the clamping device and that the voltage limitation will be ensured automaticly for turn-off of the antiparallel diodes, too.
Protection is guaranteed even in the case of failure of the driver supply voltage.

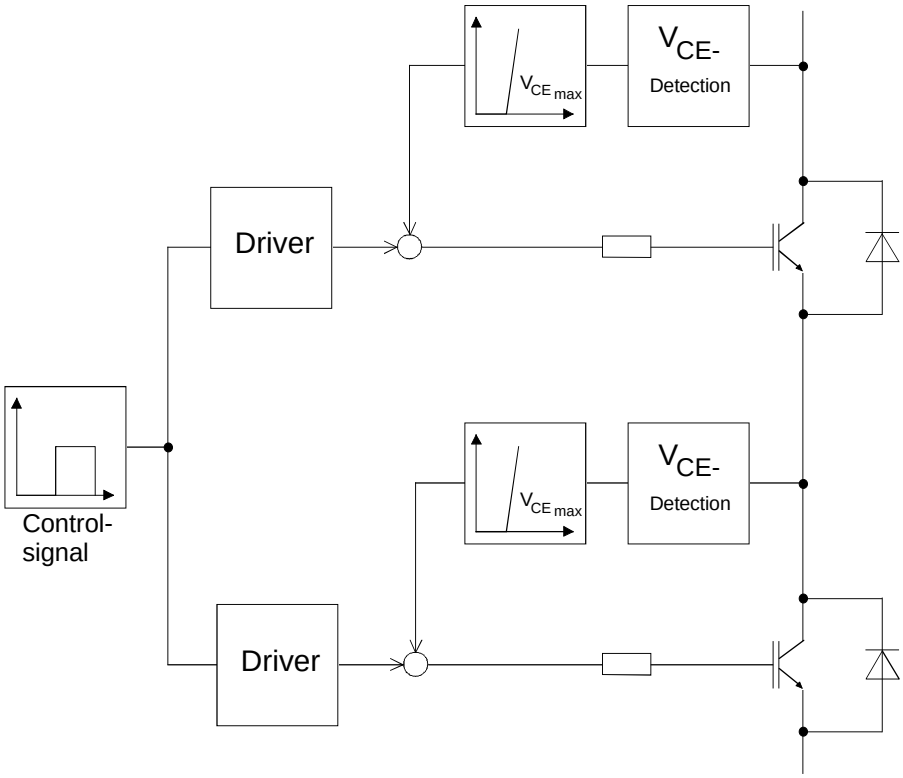

Figure 3.76 Active voltage limitation / active clamping

Master-slave conceps [110]

A modification of the commonly known master/slave principle, which originates from thyristor technology, is also applicable to dynamic voltage symmetrization (Figure 3.77).

Only the bottom switch (master) is equipped with a complete driver circuit with auxiliary power supply and potential-separated control pulse input. This is the major advantage of the principle. The driver circuit of the top switch (slave) integrates nothing but the output stage. The decoupling between master and slave is taken over by a high blocking diode. The slave will be turned on as soon as its emitter potential has dropped to a point where the decoupling diode is able to turn on, i.e. with a slight shift in time. The slave is turned off by blocking the decoupling diode. Principally, several slaves may be connected in cascade.

While this concept is able to manage turn-off symmetrization very well, turn-on symmetrization will be strongly restricted.

Therefore, a combination of the master/slave concept and active clamping is recommended.

The disadvantage of disadvantageous turn-on symmetrization can be ignored in ZVS-applications [110].

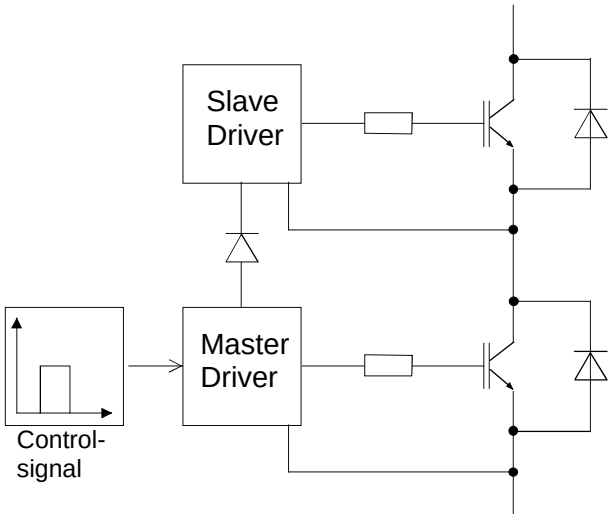

Figure 3.77 Basic principle of the master/slave concept

Conclusions

In addition to the high resistance parallel resistors for static symmetrization, passive and/or active measures to manage dynamic symmetrization must be taken when IGBT or MOSFET modules are connected in series.

Except for active clamping the variants introduced will merely protect the transistors, so that additional passive RC networks for protection of the inverse diodes will be necessary.

The combination of active clamping and a reduced RC network seems to be a good compromise for symmetrization of the switching edges with regard to circuit requirements, reliability and functionality [236].

3.8 Soft switching in ZVS or ZCS-mode / switching loss reduction networks

3.8.1 Requirements and application fields

At present, converter technology is dominated by topologies related to impressed direct voltages. IGBTs and MOSFETs are operated almost entirely in hard switching mode in these circuits, i.e. they are subject to high energy dissipation and power dissipation peaks resulting in typical switching frequencies between 3 kHz and 20 kHz (IGBTs) or 50 kHz (high voltage MOSFETs), respectively.

Increasing the switching frequency will principally lead to reduction of size and weight of passive energy stores (chokes, capacitors, transformers, filters), which is of interest, for example, with respect to the integration of transformers into converter systems.

Typical application fields:

- battery charging,
- UPS with potential-isolated DC-DC-converter,
- conventional power supplies (switch-mode power supplies),
- PFC-circuits,
- industrial power supplies (welding, electroplating, inductive and capacitive heating etc.).

If the required switching frequency cannot be attained in a hard-switch application, the resulting power dissipations have to be reduced.
Basicly, there are two ways of reducing switching losses:

1. Attachment of additional switching loss reduction networks, whilst keeping the basic circuitry.
2. Soft switching in ZVS or ZCS-mode.

3.8.2 Switching loss reduction networks

Power-electronic switches with conventional thyristors, GTOs or MCTs (MOS-controlled thyristors) require switching loss reduction networks in order to guarantee operation within the safe operating area, i.e. these networks are unavoidable if the components are to live up to their basic functions during switching mode.
In contrast to that, the SOA-characteristics of modern IGBTs and MOSFETs allow operation without the attachment of networks, and additional networks may only serve to reduce switching losses or support symmetry tasks in the case of cascading.

Figure 3.78 shows a conventional step-down converter with IGBT and simple switching loss reduction networks.

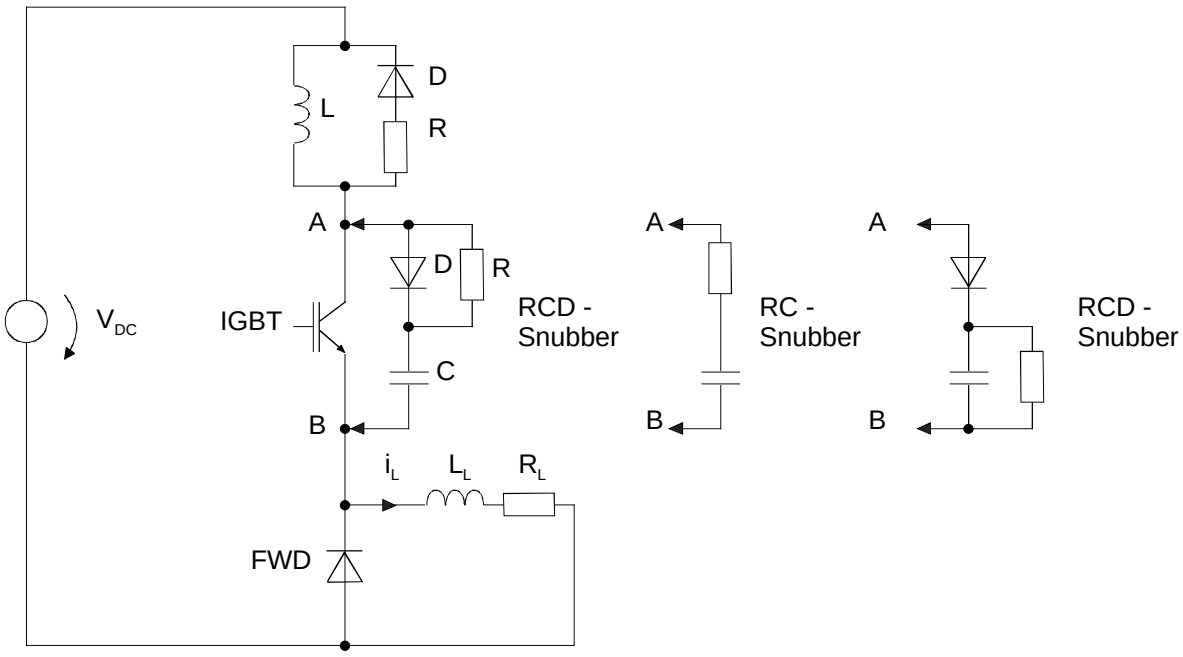

Figure 3.78 Step-down converter with IGBT and simple switching loss reduction networks

Reduction of turn-on losses (RLD-network):

At first, the IGBT is in off-state ($v_{ce} \approx v_{DC}$) and the load current is conducted through the free-wheeling circuit.
The commutation process from the free-wheeling diode to the IGBT (inductive commutation) is triggered by active turn-on of the IGBT. As soon as the network inductance has reached a certain value, it will almost completely absorb the commutation voltage (corresponds to the input DC-voltage of the converter) when the collector current rises, so that the collector-emitter voltage is quickly reduced to a very low level. At the same time, the network inductance will effect a reduction of the current commutation speed.

On consideration of both aspects, IGBT turn-on losses may be reduced substantially .
The characteristics of collector current and collector-emitter voltage correspond to soft switching as explained in chapter 0.
In chapter 3.8.3 we will demonstrate that the attachment of air coils, with ratings of only some micro-Henry, will be sufficient to reduce IGBT and MOSFET power dissipations very efficiently.
In addition to the reduction of IGBT turn-on losses, the turn-off losses of the free-wheeling diode will also be decreased during the inductive commutation, since the reduced current commutation speed will lead to low-level reverse recovery peak currents.
The combination of R-D will create a free-wheeling circuit for the snubber inductance, which will set a limit to IGBT and FWD-overvoltages during turn-off.

Recommendations for dimensioning:

1. Do not make dimensions for network inductance any higher than necessary for switching loss reduction (see chapter 3.8.3).
2. Minimize the internal snubber network inductance.
3. The relation of R and L results in a time constant (τ = L/R) necessary for internal energy discharge of the inductance. This, in turn, will result in a minimum IGBT static off-time (duty cycle limitation) to achieve efficient reduction of turn-on power dissipations (no residual current left in L). On the one hand, increasing R will result in shortening the minimum IGBT static off-time, on the other hand, however, it will effect a higher voltage and, consequently, higher power dissipations in the turned off power semiconductors.

Reduction of turn-off losses (RCD-network):

At first, the IGBT is in on-state and conducts the load current.
The commutation process from IGBT to free-wheeling diode (capacitive commutation) is triggered by active turn-off of the IGBT.
The load current quickly commutates from the IGBT to the parallel D-C-leg, by which the collector current will decrease on simultaneous reduction of the collector-emitter dv/dt.
This way turn-off losses in the IGBT will be reduced. The characteristics of collector current and collector-emitter voltage then correspond to soft switching as explained in chapter 0.
Chapter 3.8.3 will explain, among other things, that the power loss reduction effect, which is achievable at a certain capacitance, is strongly dependent on the specific structure of the transistor (MOSFET, NPT-IGBT, PT-IGBT).
At the end of voltage commutation, the free-wheeling diode will turn on with low losses and take over the snubber capacitance current.
With the next turn-on of the IGBT the energy stored by the network capacitance will be discharged by resistance R.

Recommendations for dimensioning:

1. Do not make dimensions for the network capacitance any higher than necessary for switching loss reduction (see chapter 3.8.3).
2. Use fast snubber diodes with low turn-on overvoltage (forward recovery).
3. Use pulse-proof capacitors (film capacitors etc.) with low internal inductance.
4. Minimize loop inductance of the IGBT-RCD-network.

5. The product of R and C results in a time constant (τ = R * C) necessary for internal energy discharge of the capacitance. This, in turn, will result in a minimum IGBT on-time (duty cycle limitation) to achieve an efficient reduction of turn-off power dissipations (no residual voltage left in C). On the one hand, a reduction of R will result in shortening the minimum IGBT on-time, on the other hand, it will effect a higher current and, consequently, higher power dissipations during turn-on of the transistor.

Anyway, bigger inductive and capacitive snubber elements will always lead to longer commutation times!

In pulsed circuit topologies, where inductive and capacitive commutation processes alternate within one common commutation circuit, the energy discharge in the elements L and C is subject to power dissipations during the following commutation process.
In applications using simple snubber networks, as described beforehand, the total energy stored is converted to heat mainly in the network resistor, and partially also in the transistor (dissipative snubber). Despite losses being reduced in the switches, the total efficiency of the circuit will not be improved.
Furthermore, there is a variety of low-loss snubber networks well-known from the relevant literature (non or low-dissipative snubbers), where the energy is stored in resonant circuits or fed back to the DC-link. However, such types of circuits are often very complicated to dimension, and the production of layout and circuitry is subject to a great deal of effort [258], [78].

3.8.3 Soft switching

3.8.3.1 Typical current and voltage characteristics / power semiconductor stress

Soft switching is another possibility to reduce losses in power electronic switches.
Actually, the operation of power electronic switches in ZVS-mode (zero-voltage-switch) or ZCS-mode (zero-current-switch) is called “soft switching“ (see chapter 0).
The variety of converter circuits working according to these principles is generally assigned to resonance or quasi-resonance technology.

ZVS:
- The commutation process is started by active turn-off, switching losses are reduced by parallel connection of the commutation capacitance C_K to the switch,
- the commutation process is completed by passive, low-loss turn-on at a switch voltage of $v_s \approx 0$,
- the commutation inductance L_K has been minimized.

ZCS:
- The commutation process is started by active turn-on, switching losses are reduced by series connection of the commutation inductance L_K to the switch,
- the commutation process is completed by passive, low-loss turn-off at a switch current of $i_s \approx 0$,
- the commutation capacitance C_K has been minimized.

For corresponding commutation circuits please refer to chapter 0.
Soft switching is based on the pre-condition that only one kind of commutation process - either inductive commutation/ZCS or capacitive commutation/ZVS – takes place in the commutation circuit of a converter. With this restriction the loss of one control possibility has to be accepted in comparison to hard switching .

Soft switching can only be realized, if the polarities of the driving commutation voltage v_K or of the commutated output current i_L are reversed between two commutation processes of the same kind.
In the case of commutation voltage polarity reversal, a reversed voltage is applied to the switch during off-state.
In the case of current polarity reversal, a reversed current is applied to the switch during on-state.

The currently available IGBTs, MOSFETs and diodes are designed and optimized for hard switch applications only, where they feature similar characteristics.
On the other hand, comprehensive examinations during the past few years ([433], [44]) have demonstrated that differing component structures and technologies behave differently in many aspects during soft switching (see chapter 3.8.3.3).
However, these differences, , are not recognizable by the user from the currently available datasheets.

Figure 3.79 shows an example of a low-loss converter system with ZVS and ZCS including an HF-transformer, the functions of which would be suitable for use in photovoltaic, battery charge or UPS applications.

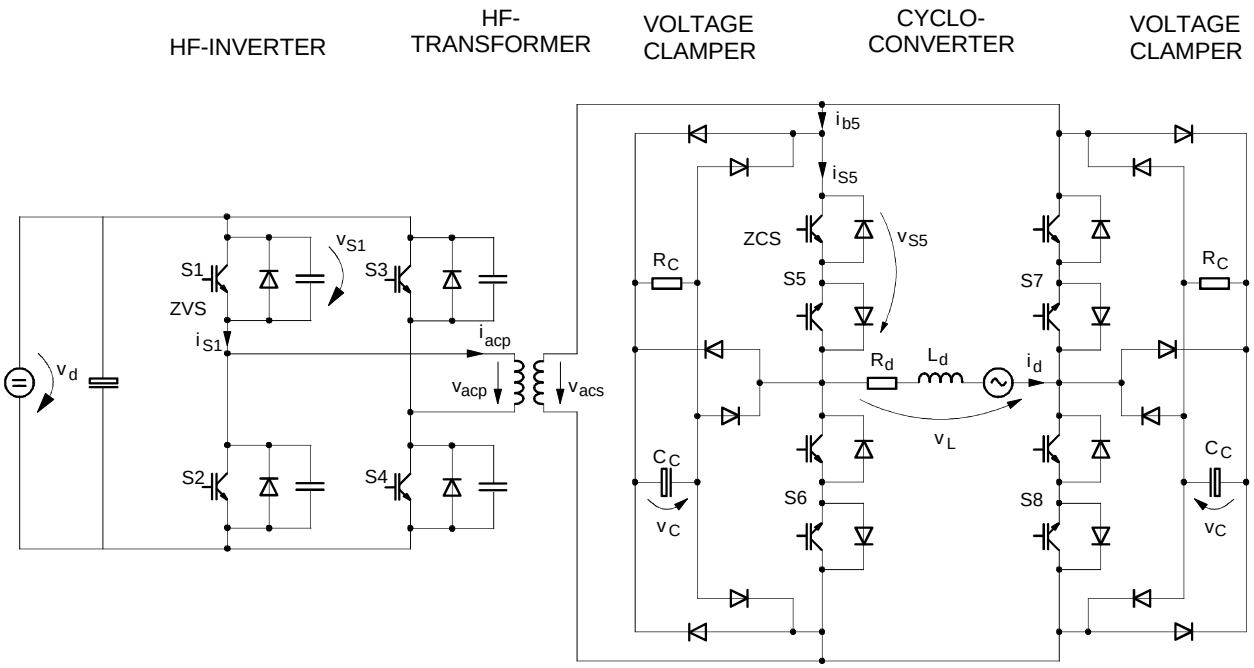

Figure 3.79 Converter system with ZVS and ZCS [49]

The system consists of a ZVS DC/AC-inverter, an HF-ferrite-transformer and a ZCS-cyclo-converter, which is able to convert the HF-alternating voltage of the transformer (e.g. 20 kHz, trapezoidal) to a low-frequency voltage (e.g. 50 Hz, sinusoidal). The time-shifted alternating switching of ZVS and ZCS guarantees permanent soft switching in the system.
Figure 3.80 shows typical current and voltage characteristics as well as stress of ZVS and ZCS with this example of an converter.

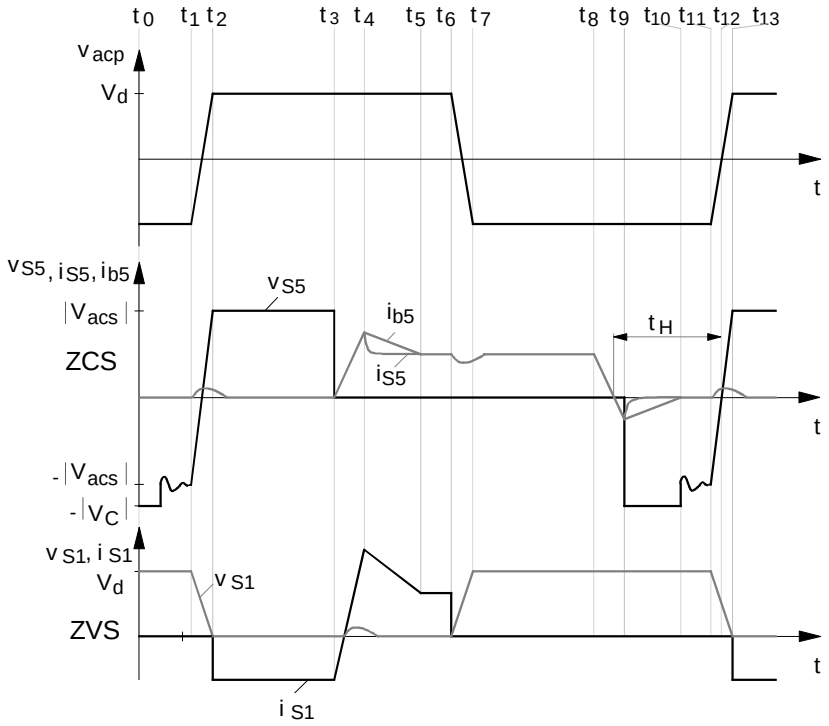

Figure 3.80 Typical characteristics for the circuit of Figure 3.79 [49]

ZVS (switch S1), 1 voltage direction, 2 current directions:

1. Passive turn-on of ZVS (diode) almost free of losses on condition that $v_s \approx 0$ at time t_2 (end of capacitive commutation process from S2 to S1),
2. Reversal of current direction within ZVS between t_3 and t_4, due to switching procedure in the cyclo-converter. The switch current which comes from the diode is impressed to the antiparallel IGBT, which is ready to take over the current - i.e. the gate is triggered - with a di/dt determined by the outer circuit. Power losses in the IGBT are caused by the process of conductivity modulation.
3. Active turn-off of ZVS (IGBT) at t_6: power dissipations during active turn-off are reduced by effectiveness of parallel commutation capacitance C_K (fast current commutation to C_K and dv_{CE}/dt-limitation).

ZCS (switch S5), 2 voltage directions, 2 current directions:

1. Active turn-on of ZCS (IGBT) at t_3: power dissipations during active turn-on are reduced by the effectiveness of series connection of the commutation inductance L_K (in this case stray inductance of transformer; fast voltage commutation to L_K and di/dt-limitation).
2. Passive turn-off of ZCS subject to switching losses with reverse-recovery-di/dt of series diode at t_9. The current in the related IGBT drops to zero. At this time, no switching losses are generated in the IGBT.
3. Reversal of voltage direction at ZCS between t_{11} and t_{13}, due to switching in the DC/AC-inverter: the switch voltage which comes from the diode connected in series to the IGBT is impressed with a dv/dt determined by the inverter.
   Power dissipations generated in the IGBT are due to discharge of the residual storage charge left in the n^--base. The losses are mainly determined by the time difference t_H (called hold-off time) as well as by the charge carrier lifetime.
   If the hold-off times are very short, the losses arising can be compared to tail current power dissipations during hard switching.

3.8.3.2 Requirements on semiconductor switches and their drivers

ZVS:

Power semiconductors:

- have to feature active turn-off and good power-loss reduction behaviour during turn-off,
- for IGBTs: - short charge carrier lifetime,
  - minor influence of junction temperature on tail charge and charge carrier lifetime,
- low forward turn-on overvoltage during conductivity modulation with zero-voltage turn-on and impressed di/dt,
- since ZVS-diodes do not turn off with reverse-recovery-di/dt and take on reverse voltage at the same time, there are only small requirements to their reverse-recovery behaviour compared to hard switching.

Driver circuit:

The driver circuit has to comply with the following minimum requirements:

- active turn-off of IGBT/ MOSFET and
- switch voltage monitoring and passive turn-on of ZVS at $v_S \approx 0$ V.

Modified ZVS-mode:

The duration of a capacitive commutation process can be approximated as follows:

$t_{Kc} \approx (C_K * v_K)/i_L$

Explanations: C_K: commutation capacitance (power loss reduction capacitance),
v_K: commutation voltage,
i_L: load current to be commutated.

With low load currents, the commutation process in power converters may last an undesirably long time, which might endanger faultless operation of the circuit. This can be avoided by application of modified zero-voltage-switches, which will break off the commutation process after an adjustable maximum commutation time by active turn-on towards the not yet completely recharged commutation capacitance. However, this bears the consequence of increased switching losses.

Figure 3.81 shows the principle operation of a modified ZVS.

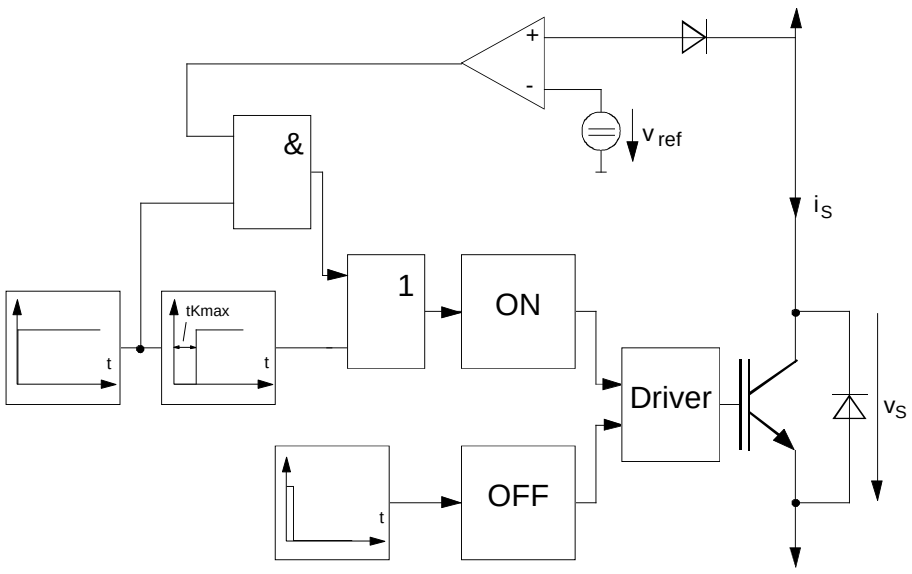

Figure 3.81 Principle of a modified ZVS

ZCS:

Power semiconductors:

- have to feature active turn-on and good power-loss reduction behaviour during turn-on,
- low power semiconductor capacitance
- for IGBTs: - short charge carrier lifetime,
  - minor influence of junction temperature on tail charge and charge carrier lifetime,
- short dynamic saturation periods during turn-on
- diodes: low reverse recovery charges.

Driver circuit:

The driver circuit has to comply with the following minimum requirements:

- active turn-on of IGBT/ MOSFET and
- switch current monitoring and passive turn-off of the ZCS at $i_S \approx 0$ A.

Modified ZCS-mode:

The duration of an inductive commutation process can be approximated as follows:

$t_{Ki} \approx (L_K * i_L)/v_K$.

Explanations: L_K: Commutation circuit inductance (power loss reduction inductance),
v_K: commutation voltage,
i_L: load current to be commutated.

With low commutation voltages or high load currents, the commutation process in power converters may last an undesirably long time, which might endanger faultless operation of the circuit. This can be avoided by the application of modified zero-current-switches, which will break off the commutation process after an adjustable maximum commutation time by active turn-off towards the still live commutation inductance. However, this bears the consequence of increased switching losses. Furthermore, zero-current-switches have to be equipped with an overvoltage protection in almost any application (see also Figure 3.79 and chapter 3.6.3).
Figure 3.82 shows the principle operation of a modified ZCS.

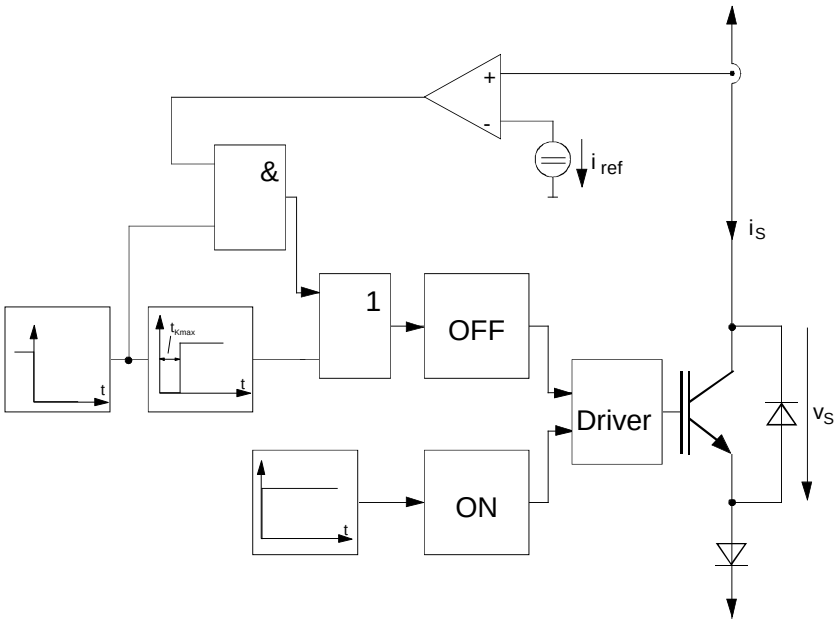

Figure 3.82 Principle of a modified ZCS

3.8.3.3 Features of switches

ZVS with PT- and NPT-IGBTs [43], [49]

zero-voltage turn-on with impressed di/dt

Before the IGBT is able to conduct a current, it has to be turned on by the driver. Since conductivity modulation within the n^--base will not have taken place before the current is taken over, the IGBT will react to the di/dt-impression by transient increase of the on-state voltage and, thus, by increased on-state losses at this time interval (forward recovery). Dynamic overvoltage, duration of conductivity modulation and, consequently, power dissipations depending mainly on the basic doping of the n^--base, emitter efficiency, charge carrier lifetime, di/dt, switch current final value (load current) and temperature.
NPT-IGBTs, which are characterized by low emitter efficiency and long charge carrier lifetime, will respond by relatively low forward voltage peaks (Figure 3.83). However, the procedure, may take more than 10 µs.
By contrast, the transient forward voltage peaks of PT-structures exceed the stationary forward voltage by 30 to 40 times (high emitter efficiency, short charge carrier lifetime). However, this procedure will only take some 100 ns (Figure 3.83b). The contrary tendency of voltage peak and process duration will result in a certain alignment of power dissipations of NPT and PT-IGBT-ZVS, which may contribute substantially to the total power dissipation in high-switching-frequency applications (Figure 3.84a and b).

If the ZVS-short-circuit protection is based on a v_{CE}-evaluation, it has to be gated during di/dt-impression to avoid breakdown of the converter.

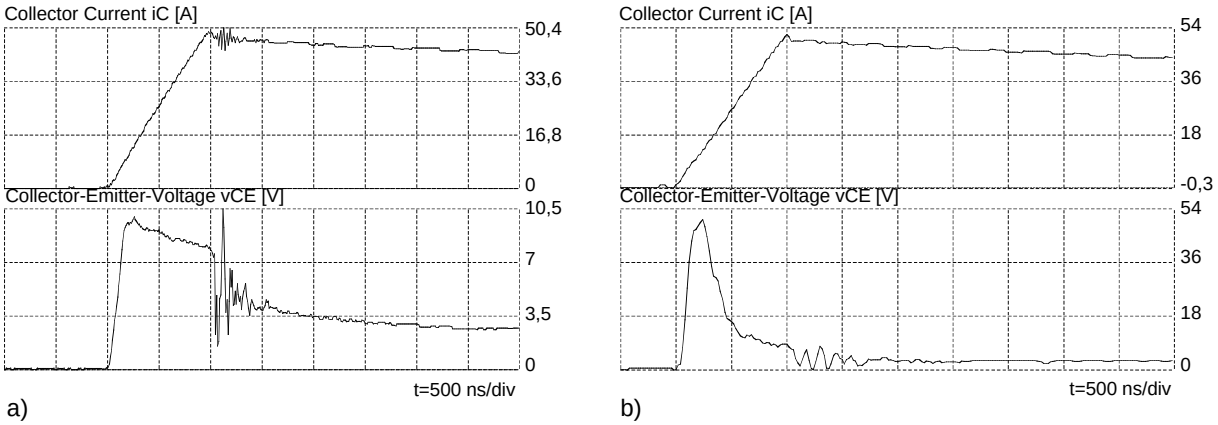

Figure 3.83 a) di/dt-impression in a 1200 V/50 A-NPT-IGBT (di/dt = 50 A/µs; i_L = 50 A)
b) di/dt-impression in a 1200 V/50 A-PT-IGBT (di/dt = 50 A/µs; i_L = 50 A)

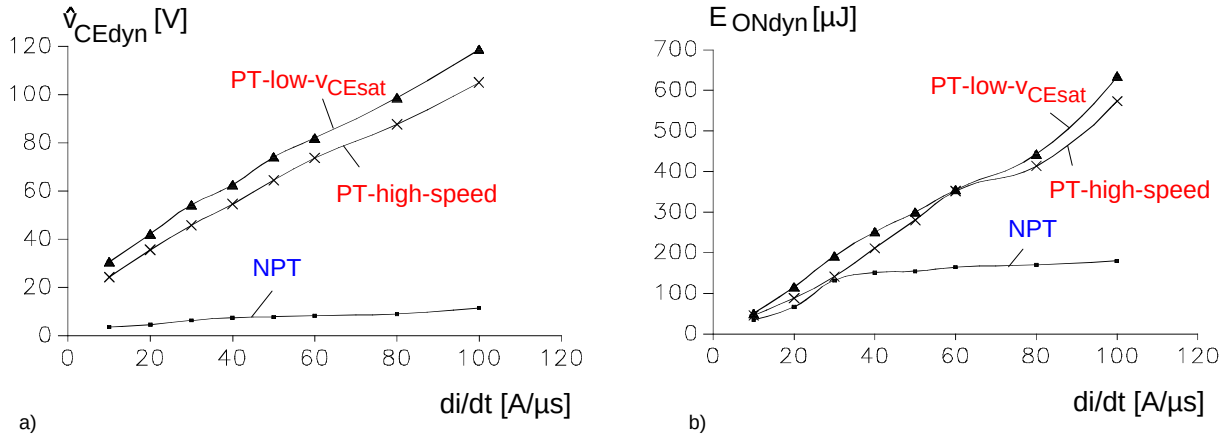

Figure 3.84 a) Dynamic forward voltage amplitude of 1200 V/50 A-NPT and PT-IGBTs versus impressed di/dt (i_L = 30 A, T_j = 30°C)
b) Power dissipations during di/dt-impression of 1200 V/50 A-NPT and PT-IGBTs versus impressed di/dt (i_L = 30 A, T_j = 30°C)

active, low-loss turn-off

During active low-loss turn-off the IGBT current can be commutated directly to the paralleled capacitance C_K with reduced collector-emitter dv/dt, which provides reduced switching losses. The tail current characteristic, i.e. discharge of charge stored in IGBT after blocking of MOSFET-channel, is substantially determined by the collector-emitter dv/dt. Increasing the commutation capacitance will lower the initial tail current value (comparable to a capacitive current devider between IGBT and snubber capacitor). At the same time, the tail current will be prolonged, which impairs the reduction of turn-off losses. For NPT-structures with long charge carrier lifetime this will lead to unsatisfactory switching loss reduction (Figure 3.85a, Figure 3.86). On the other hand, the oscillogram in Figure 3.85b shows that with PT-structures the tail current may already have dropped to zero before the collector-emitter voltage has reached the level of the outer commutation voltage. The result of tests with 1200 V/50 A -PT-IGBT-modules was that at a commutation capacitance C_K = 30 nF, turn-off switching losses may be reduced by 50 % compared to hard switching (Figure 3.86). With NPT-IGBTs switching losses could be reduced by merely 20 %.

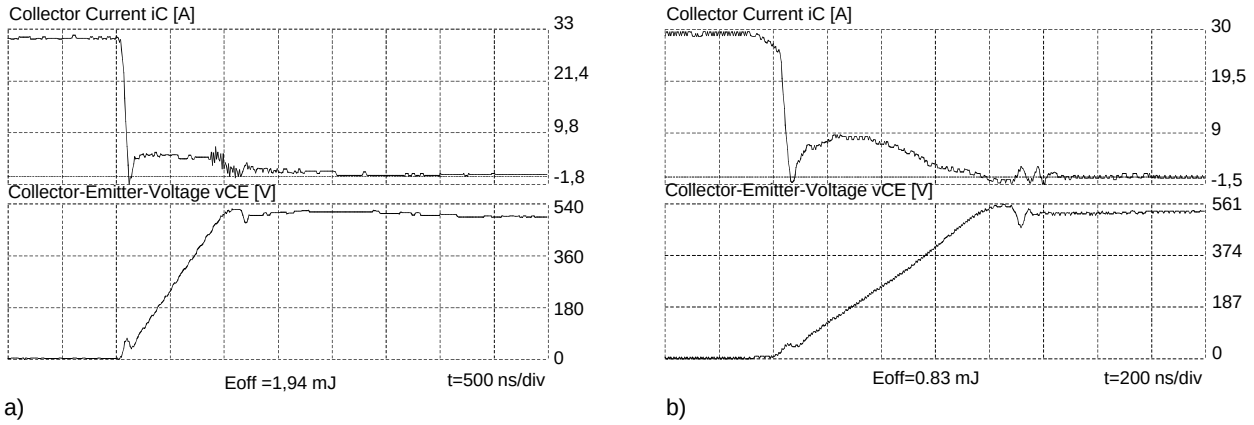

Figure 3.85 a) Low-loss turn-off of 1200 V/50 A NPT-IGBTs at C_K = 47 nF
b) Low-loss turn-off of 1200 V/50 A PT-IGBTs at C_K = 30 nF

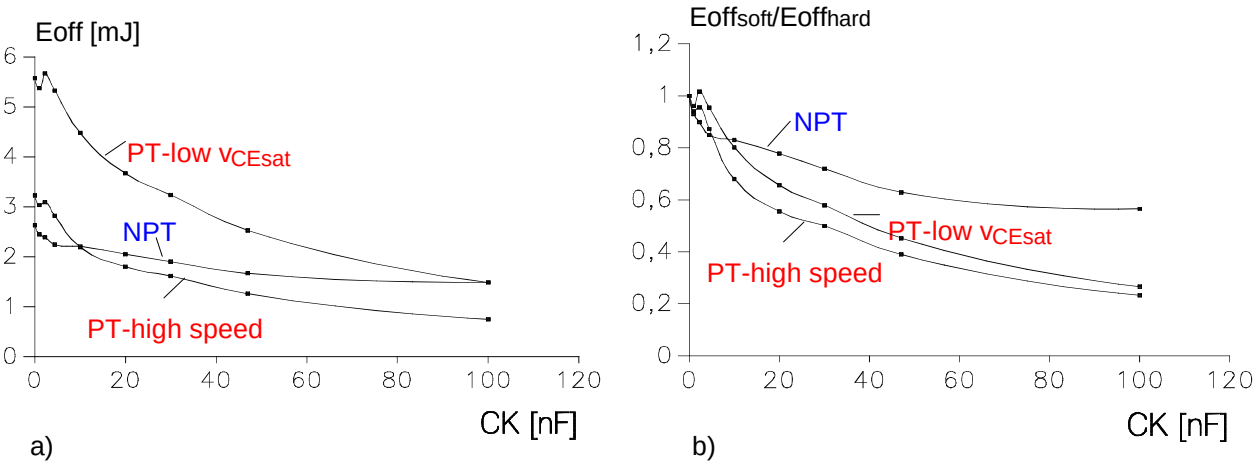

Figure 3.86 a) Turn-off power dissipations of 1200 V/50 A-IGBTs versus commutation capacitance C_K (v_K = 500 V; i_L = 50 A; T_C = 80°C)
b) Turn-off power dissipations related to hard switching of 1200 V/50 A-IGBTs versus commutation capacitance C_K (v_K = 500 V; i_L = 50 A; T_C = 80°C)

ZVS with MOSFETs, [43]

MOSFETs are unipolar devices which should not be charged or discharged with any storage charges. This results in the following special features for use in ZVS:

- There is no dynamic forward overvoltage during zero-voltage turn-on with impressed di/dt.
- Within the same class of devices the comparison to IGBTs shows that switching losses in MOSFETs with commutation capacitances of some nF may be almost completely avoided during turn-off. This is also supported by the relatively high output capacitance of MOSFETs in the commutation circuit,
- The process, where the off-state transistor is subject to high dv_{DS}/dt, which is critical for MOSFETs (see chapter 3.5), does not exist in ZVS-mode.
  Therefore, MOSFETs may be driven principally by negative gate-source voltage.

Fast diodes in ZVS

Fast diodes in ZVS feature the following special characteristics:

– In ZVS diodes will not turn off with reverse-recovery-di/dt at simultaneous take-over of reverse blocking voltage. The reverse-recovery behaviour of fast diodes is therefore negligible compared to hard switching.

However, optimized dynamic turn-on is still required in ZVS-applications. In this respect, the use of CAL-diodes is of special advantage (see chapter 1.3).

ZCS with PT- and NPT-IGBTs [44], [49], [146]

active, low-loss turn-on

Figure 3.87 shows the oscillogram of low-loss turn-on of a 1200 V/50 A –NPT-IGBT as well as the dependence of turn-on losses of different power semiconductors on the commutation inductance L_K. It becomes clear that IGBTs and MCTs, respectively, are capable of optimized switching loss reduction. Power dissipations compared in the IGBTs and MCTs are almost identical at a commutation inductance of only 3µH and, as for IGBTs, they amount to merely about 15 % compared to hard switching.
In contrast to turn-off during ZVS-mode, PT- and NPT-IGBTs can be turned on with equal optimal loss reduction.
Power dissipations occurring during turn-on of IGBTs in ZCS-mode are caused by the processes during dynamic saturation.

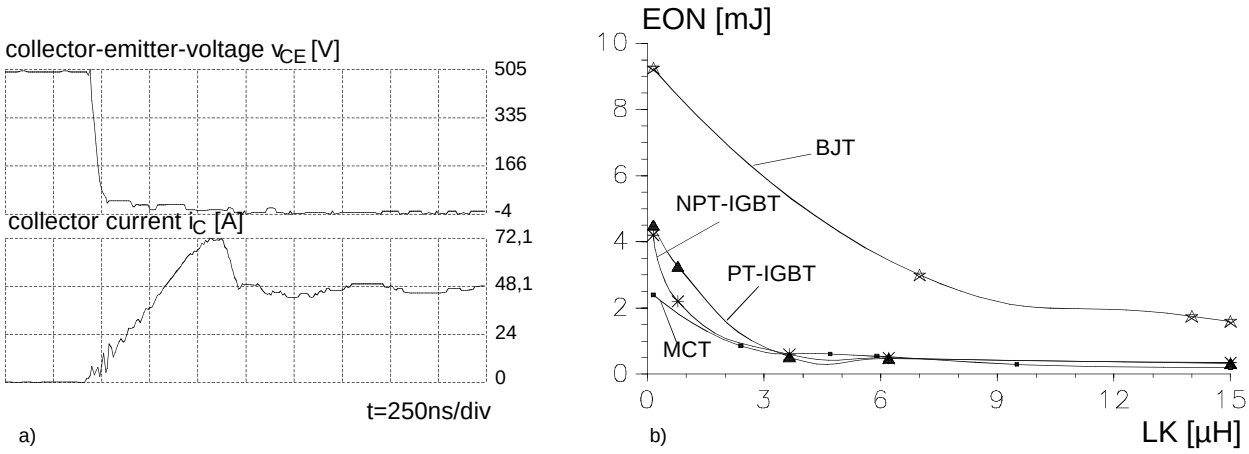

Figure 3.87 a) Low-loss turn-on of NPT-IGBT (L_K = 3.6 µH)
b) Turn-on power dissipations of ZCS as a function of the commutation inductance L_K (v_K = 500 V, i_L = 30 A, T_j = 30°C)
BJT = Bipolar Junction Transistor, MCT = MOS-Controlled Thyristor

Voltage reversal in turned off ZCS with removal of residual IGBT storage charge

Figure 3.88 shows the processes involved in passive turn-off of IGBT-ZCS (IGBT with series and antiparallel diode) with subsequent change of the switch voltage polarity.
It becomes clear that, with PT-structures the residual charge to be removed is low (short charge carrier lifetime) when the IGBT takes on forward blocking voltage after the hold-off time which will reduce power dissipation during this process.

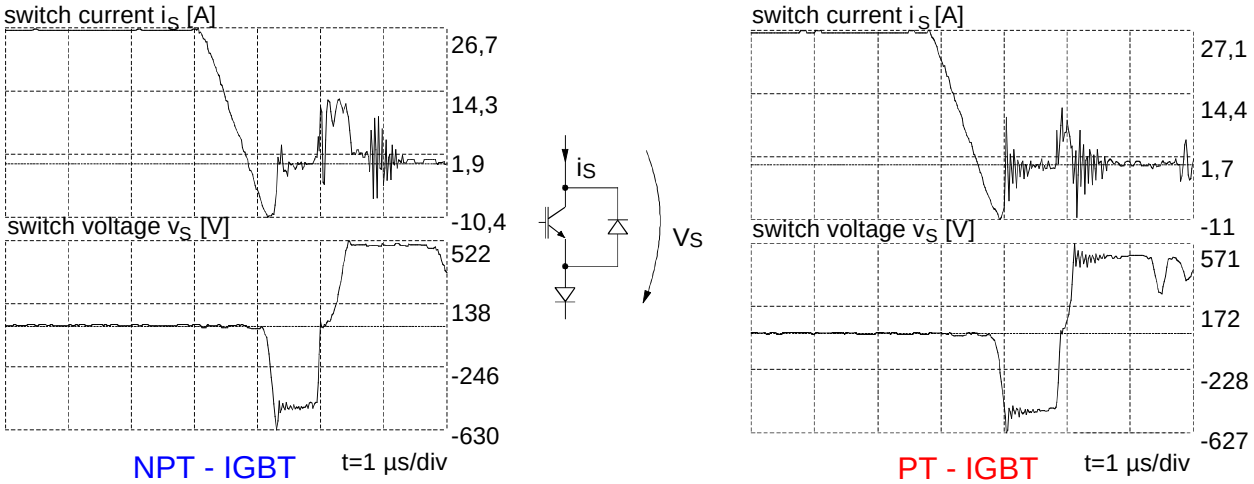

Figure 3.88 Turn-off characteristics of 1200 V/50 A-NPT and PT-IGBTs (t_H = 1.3 µs, L_K = 10µH)

The dependence of residual storage charge on hold-off time is shown in Figure 3.89a. Here, the advantages of PT-structures are illustrated very clearly. On the contrary, storage charges of PT-structures are more temperature-dependent, which restricts the maximum switching frequency due to the risk of thermal instability especially in the case of short hold-off times (Figure 3.89).

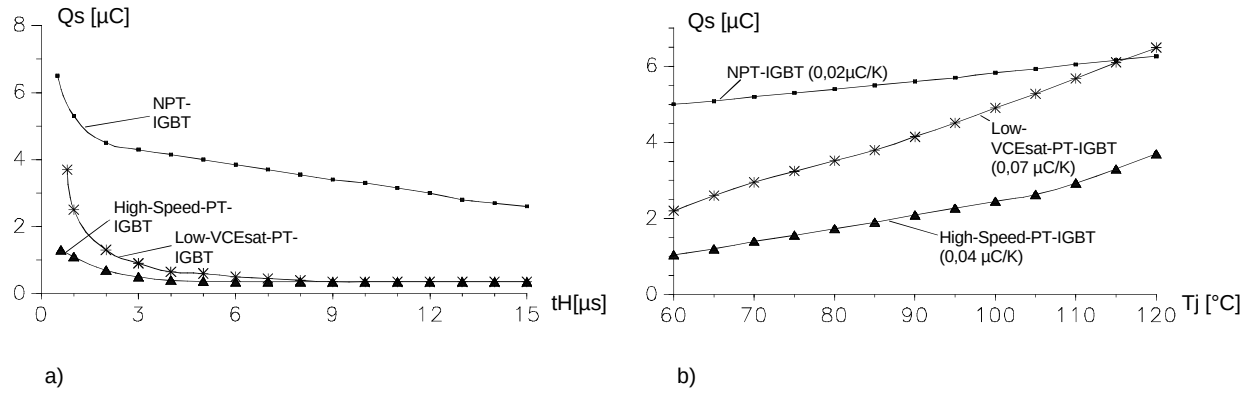

Figure 3.89 a) Residual storage charge of PT and NPT-IGBT-ZCS as a function of hold-off time (v_K = 400 V, i_L = 30 A, L_K = 10µH, T_j = 60°C)
b) Storage charge of PT and NPT-IGBT-ZCS as a function of the transistor junction temperature (v_K = 400 V, i_L = 30 A, L_K = 10 µH, t_H = 1.3 µs)

An IGBT-ZCS-driver circuit is introduced in [44], where an additional collector current is fed to the IGBT by the driver during hold-off time to remove the storage charge. This measure had proven to effect a drastic reduction of power dissipations during blocking voltage take-on, especially for hold-off times t_H > 2 µs.

ZCS with MOSFETs

The following special features have to be considered when using MOSFETs in ZCS:

– Since MOSFETs do not feature dynamic saturation, MOSFETs with very small (...1 µH...) series power-loss reduction inductances may almost be relieved completely of turn-on losses. However, the high output capacitance (typical for MOSFETs) will have negative effects on turn-on power dissipations. If high switching frequencies are applied (> 50 kHz), the resulting share of power losses has to be considered as a part of the total power dissipation.

– Due to the unipolarity of MOSFETs there will be no removal of residual storage charge during change of polarity of the switch voltage at the end of hold-off time. On the other hand, the relatively high output capacitance has to be recharged.

Fast diodes in ZCS

The following special features have to be considered:

– Diodes in ZCS will turn off with reverse-recovery di/dt at simultaneous take-on of reverse-blocking voltage. Due to the existing commutation inductances, current will be commutated in the diode at a lower speed compared with hard-switching converters (lower reverse current peak, reduced turn-off losses).
– The use of fast diodes as series diodes of IGBTs or MOSFETs in ZCS requires very good dynamic turn-on behaviour of the diodes (see chapter 1.3).

3.8.3.4 Conclusions

The behaviour of IGBTs during hard switching is not applicable to soft switching. In principle PT-IGBTs with a shorter charge carrier lifetime are more suitable for soft-switching applications than NPT-IGBTs due to the dynamic processes explained before. This had been proven in tests with 1200-V-switches by substantial reduction of total power dissipations in PT-IGBT-switches.

This comparison may not be transferred to other voltage classes. For new 600 V-devices the result may be in favour of NPT-structures in case thin-wafer technologies are applied (reduced forward voltage drop and carrier charge) due to the improved temperature-stability of the device parameters.

MOSFETs - especially when used as ZVS - are preferred for soft-switching applications due to their unipolar character.
Because the foward losses are high by principle, application at high switching frequencies (> 50 kHz) as well as in the low voltage/ high current range is recommended.
New MOSFET-technologies with decreased R_{DSon}-values (e.g. CoolMOS) provide even more fields of application.

Since there is a variety of low-loss converter topologies with specific requirements to switches, a standard conclusion on the limitation of frequencies of IGBT and MOSFET switches cannot be drawn.

In the exemplary circuit in Figure 3.79 the following realistic maximum frequencies are given for 1000..1200 V/ 20..50 A- devices:

NPT-IGBT:	ZVS:	50 kHz	ZCS:	70...80 kHz
PT-IGBT:	ZVS:	70...80 kHz	ZCS:	80...90 kHz
MOSFET	ZVS:	> 200 kHz	ZCS:	> 200 kHz

3.9 Handling of MOSFET, IGBT, MiniSKiiP and SKiiPPACK modules

3.9.1 Sensitivity to ESD and measures for protection

All MOSFET or IGBT power modules are sensitive to ESD (**E**lectro **S**tatic **D**ischarge) because the thickness of the gate isolation only amounts to some ten nanometers.
The degree of sensitivity is dependent on the input capacitance value (MOSFET: C_{GS} gate-source capacitance/IGBT: C_{GE} gate-emitter capacitance).
IGBTs and power MOSFETs with big chip areas are characterized by high input capacitances and are classified as minor sensitive compared to small-signal components according to standard MIL-STD 883C, procedure 3015.6.

With respect to the handling of IGBT or MOSFET power modules, the specifications of the MIL-standard mentioned above as well as of standard DIN VDE 0843 TS, which is identical to IEC 801-2, must be adhered to.
Inspection and further processing should be carried out only at specially prepared workplaces with conductive tables, ground connections etc. by suitably dressed staff (antistatic overalls, wrist strap, if available). All transportation and assembly equipment as well as PCBs have to be adjusted according to the requirements of ESD-sensitive components before they are subjected to further processing.

The power modules are delivered with gate and source terminals (MOSFET) or gate and emitter terminals (IGBT) short-circuited by conductive foam or rubber, self-sealing copper sheet, a pushed-on annular rivet or suitable conductive packaging system. As far as possible, this short circuit should be removed not until connecting the gate.

3.9.2 Mounting instructions

For the sake of optimal thermal connection between power module and heatsink, module base plate and heatsink surface must be clean and dust-free. The heatsink roughness should not exceed 10 µm (MiniSKiiP and SEMITOP: 6.3 µm), flaws must not contribute to an unevenness of more than 20µm for a distance of 10 cm.

Before the power module is mounted to the heatsink, a very thin (30...50 µm) and homogeneous layer of thermal paste has to be applied to both mounting surfaces by means of a rubber roller, for example.
For SEMIKRON power modules we recommend the use of thermal paste P12 (by Wacker Chemie), which, however, contains some silicone. Another suitable silicone-free paste is, for example, WLPF5 (by Fischer-Elektronik).

For the selection of connecting and fixing screws please refer to the following:
- assembly with washer and spring ring or crinkle type spring washer;
- minimum and maximum length of connecting screws according to module drawing and arrangement of busbars;
- minimum strength given in databooks or resulting from required mounting torque;
- surface finish and corrosion resistance.

Suitable multiple purpose screws with non-detachable washers and spring rings are available by SEMIKRON on request.

The torques indicated in the datasheets must be considered on assembly with screws. At first, the mounting screws should be tightened diagonally at about half the torque, and with full torque afterwards, using the same sequence. Due to subsidence of thermal paste, the screws should be tightened up after a few hours.

With regard to solder contacts please refer to the solder specifications in the datasheets.

For the assembly of MiniSKiiPs please ensure that the contact pads on the PCB do not show any inadmissible tin bulges, which might neutralize the spring effect. If necessary, the pads should be covered during flow soldering.
If a no-clean-flux is used, cleaning of the PCB can be omitted.

3.9.3 SKiiPPACK: thermal testing ex works [265], [93], [233]

SKiiPPACK-modules are delivered with heatsink; the module manufacturer guarantees proper assembly and optimal layout of thermal connections.
The final functional test comprises a complete heating procedure to check thermal connections.
This will avoid assembly problems at the customer and guarantee high reliability ”ex works”.

3.10 Dimensioning software

3.10.1 Model levels of mathematical circuit description

Actually, dimensioning of circuits with power semiconductors is identical to the commutation circuit layout. If the connecting parameters of the commutation circuits can be defined very clearly, considering all possible spreads, the layout can be determined very easily. In order to limit a system to the parameters of its commutation circuit, the system design has to be more comprehensive to aim at clear ratings of connecting parameters. Regarding a converter system, the final layout of control unit, main energy buffers and substantial filter elements have to be determined before dimensioning the power semiconductor environment and cooling system.
Such a top-down system design automatically requires the use of different model levels with contrary system extent and model intensity (Figure 3.90).

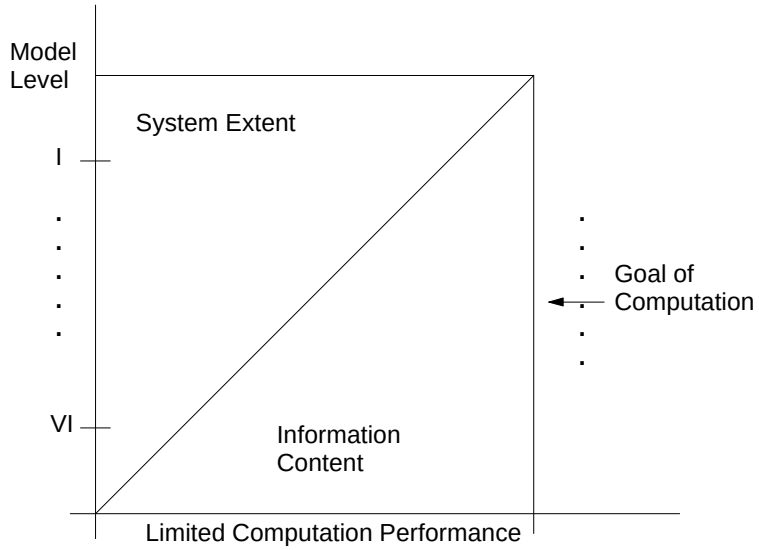

Figure 3.90 Relation between model level, system extent and information content

The information content of a model level determines, at the same time, the possible goals of computation. Figure 3.91 shows a survey of the different model levels of circuit computation. Since the switch network is the dominating part of a converter system, model levels are aligned with the kind of mathematical consideration of the switching processes.

linearized average model (model level I)

By linearization in one operating point, multiple linkages between steady values and non-linear characteristics are replaced by linear correlations. The system is then described by a linear differential equation system, which is valid for only a sufficiently small tolerance around the operating point. This level of approximation is applicable to examinations of the total system stability including control circuits, as long as there are no limitations and all steady values are monitored and kept with regard to deviations from the operating point. Comprehensive simulation system software originating from automatic control technology is available. In this respect, the efforts necessary for linearization by Taylor polynomials must not be underestimated.

non-linear average model (model level II)

If the transfer behaviour of a power-electronics basic circuit is described by the transformed average steady values ignoring switching functions, the non-linear average model will be the result. The average values or fundamental harmonics are related to the period duration of the power semiconductor switching frequency. The continuous or sampled control function is multiplicatively linked to the steady values to be transformed. Especially if the transformation relations are definite (pulsed circuits, continuous mode), the system can be described most efficiently at this model level, if the influence of the pulse frequency may be ignored. The results are valid on condition that there is an infinitely high pulse frequency, and the approximation is relatively accurate, if the steady values do not change considerably during one pulse frequency period. Also in this case, simulation programs oriented towards automatic control technology are recommended as software.

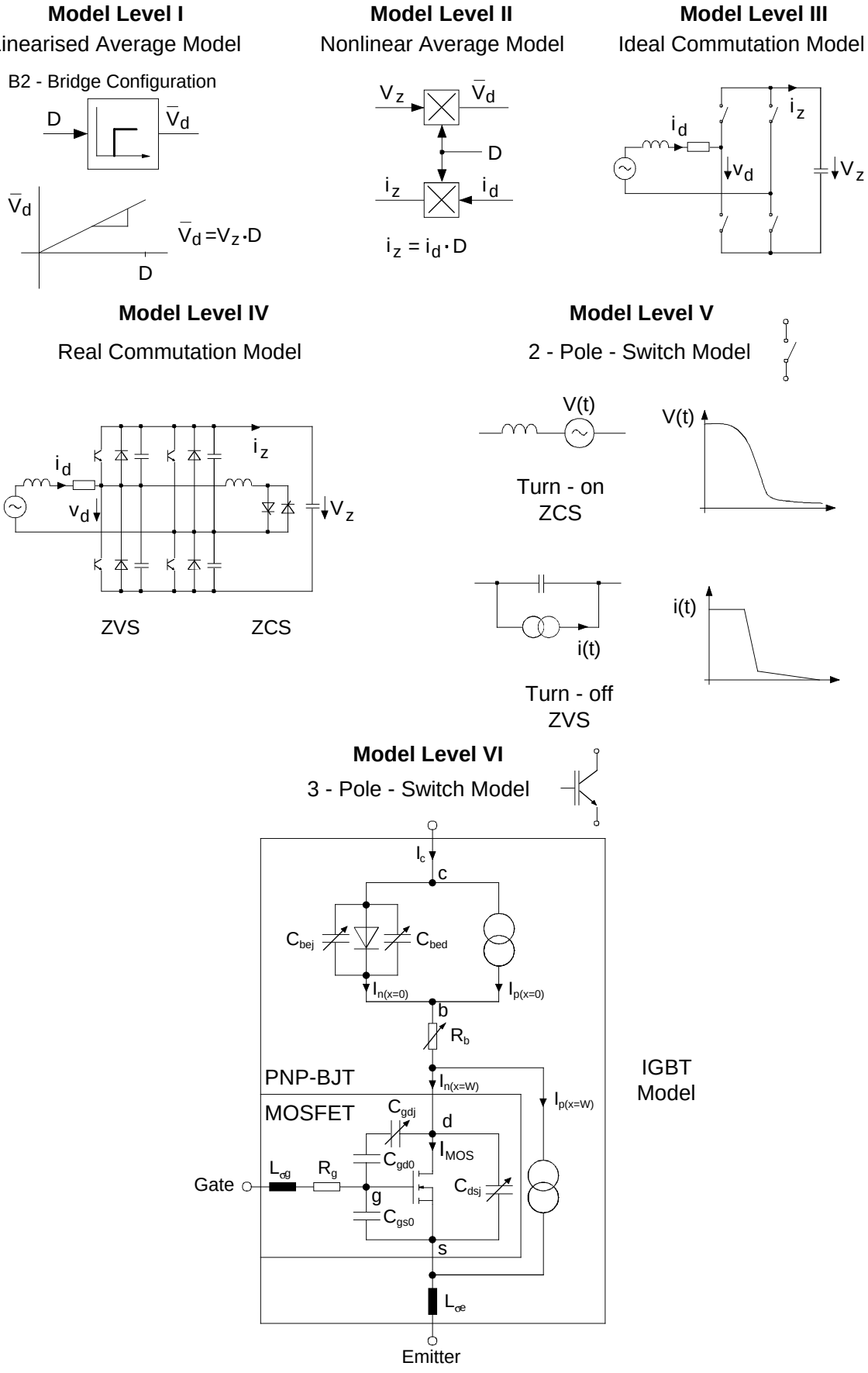

Figure 3.91 Model levels for circuit computation

ideal commutation model (model level III)

This model level is based on an idealised chopper function. Switching as well as current and voltage commutation procedures run in an infinitely short period of time. Regarding the equivalent commutation circuit, this means that commutation inductances and capacitances will be neglected. Since switching and commutation times are short compared to the pulse period duration in hard switching applications, this model level gives quite accurate results especially for hard switching basic circuits. Direct control functions are now turning to discrete control functions, or they have to be generated by the converter control unit from the quasi-continuous input control parameters according to the control principle of the switch network. The continuous or sampling system description, which is still feasible by average models, can be only partly utilized due to the switching function. Any switch state alteration, which is dependent on control or system procedures, will lead to a sequence of system states, any of which is to be described by a separate equation system. Numerically, two different methods have developed. The first, which is state-oriented, calculates the individual equation system of the current state with minimum ordinal number. The second, which is network-oriented, describes the switch network with a uniform equation system with process-dependent changing of parameters. In both cases a numeric time-step control with event detection and consideration function will be required. Both methods feature specific advantages and disadvantages.

real commutation model (model level IV)

The real commutation model is based on consideration of elements in the commutation circuit. In circuits with zero-voltage and zero-current-switches especially, the commutation time may no longer be ignored with reference to the period duration of the switching frequency. Switching times continue to be ignored. Whereas commutation is started by an active control signal, it is finalized by passive processes in the electrical network (zero-current or zero-voltage-crossing). Consideration of control parameters by a continuous or sampling control system as well as converter control unit and numeric description of the complete circuit is realized by the same methods as in the ideal commutation model.

2-pole-switch model (model level V)

This model level is applied if switching times of power semiconductors during real commutation can no longer be ignored. In resonant or quasi-resonant basic circuits especially, it is of decisive importance to the overall function that all conditions of resonance are obeyed. Since attenuation of the resonant circuits is mainly determined by the switching losses of the power semiconductors, the 2-pole-switch model comprises zero-current or zero-voltage-switches by current or voltage sources with fixed time functions during switching. These time functions are subject to experimental determination with reference to the specific operating point. Other than with the real commutation model, detection of time transition between switching and commutation process is required in case of 2-pole-switch model.

3-pole-switch model (model level VI)

At this model level, the state parameters are described by continuous functions, since the power semiconductor characteristics are realized by an equivalent network with consideration to the control input. The system may only be impaired by discontinuities resulting from the driver control leads. Therefore, system description at this level demands a model library, which comprises all power semiconductors used including active components of, at least, the driver output units. Semiconductor models consist of concentrated passive elements and active current

and voltage sources. Exact parameters are only determinable by comprehensive measurements and data by the semiconductor manufacturer. Due to the system extent this model level will mostly be restricted to the calculation of single switching frequency periods. Therefore, it is to be regarded as an efficient aid for switch dimensioning, which is less suitable for system optimization. Numerically, we always recommend using a network-oriented method due to the high number of nodes in the electrical circuit.

When selecting simulation software, the goal of computation and the resulting model level have to be clearly defined. Simulation tools which are equally suitable for all model levels do not exist. State and control or sample parameters in model levels I and II are constant, which makes them applicable to description methods used in the field of control techniques. There is a variety of simulation tools for this field of application. Model level VI is tailored towards the calculation of electrical networks and is offered by a number of suppliers in many variants. As for the model levels in between, the specialties of the varying state and control parameters have to be taken into consideration, which requires a special numeric realization of time-step control and event detection.

3.10.2 SEMIKRON software service

SEMIKRON offers a variety of possibilities to calculate and simulate many kinds of different circuits and load conditions to give application support for power modules, especially for SKiiPPACK and MiniSKiiP. The most important tool available for the customer is the program package *SKiiPsel*, which is, however, restricted to the calculation of SKiiPPACKs and MiniSKiiPs [273], [274], [276].
SKiiPsel is available on the SEMIKRON-CD-ROM [265].
This program offers the customers using SKiiPPACK and MiniSKiiP-components the possibility of determining IGBT and diode power losses in important voltage-supplied circuits on condition there is sinusoidal output current based on fixed driving conditions.

Development of the program was mainly based on user-convenience with respect to simple user interface, useability of program without additional training and fast “assessment“ of the components for its application requirements.

Based on the operating conditions to be entered (current, voltage, frequency, load cycle, temperature) the program is able to calculate power losses in the IGBTs and free-wheeling diodes and the resulting chip and heatsink temperatures.
The program will select a suitable component by means of selection criteria determined by the user, and it will check the suitability of the customer’s circuit arrangement.
With respect to cooling conditions, the user is free to choose specific options or to select those stored in the program (air or water cooler, rate of flow of coolant).

Calculation results are given graphically and as a report via ACCESS. Results about the temperature cycles under the calculated load conditions set up by the program will make assessments of the expected power semiconductor lifetime possible.

SKiiPsel works with simple characteristic models based on measured and interpolated dependencies.
The characteristics required for IGBT and diode chips used in SKiiPPACKs and MiniSKiiPs are shown below:

$V_{CE} = f(I_C)$ (IGBT) $V_F = f(I_F)$ (diode)
$V_{CE} = f(T_j)$ $V_F = f(T_j)$

and power losses in IGBT/ free-wheeling diode arms

$E_{on} = f(I_L)$ $E_{off} = f(I_L)$
$E_{on} = f(T_j)$ $E_{off} = f(T_j)$

generated when
- the SKiiPPACK is driven by the integrated driver
- the MiniSKiiP is driven according to recommendations given in the databook.
They are stored in the program and are not accessible to the user.

IGBT and diode power losses are calculated iteratively depending on output current, chip temperatures and cooling conditions according to the principle described in chapter 3.2.

MathCAD
Another possibility of application support is the calculation of circuits with non-sinusoidal output currents and conventional IGBT or MOSFET modules, which are not included in the SKiiPsel database. For this, SEMIKRON has developed a special program package based on MathCAD, which is able to produce thermal simulations of any customer circuit, e.g. buck and boost converters, current source inverter systems and line commutated converter topologies.
Apart from maximum ratings and characteristics of SEMIKRON power semiconductors the internal database contains, for example, data on heatsinks and experimental results of load cycle testing with power modules.
Therefore, calculations on temperature cycling and component lifetime are possible for any load cycles.

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